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EDITORIAL NOTICES

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The Digital Computer Newsletter, although a Department of the Navy publication, is not restricted to the publication of Navy-originated material. The Office of Naval Research welcomes contributions to the Newsletter from any source. The Newsletter is subjected to certain limitations in size which prevent publishing all the material received. However, items which are not printed are kept on file and are made available to interested personnel within the Government.

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The Office of Naval Research welcomes contributions to the Newsletter from any source. Your contributions will provide assistance in improving the contents of the publication, thereby making it an even better medium for the exchange of information between government laboratories, academic institutions, and industry. It is hoped that the readers will participate to an even greater extent than in the past in transmitting technical material and suggestions to the editor for future issues. Material for specific issues must be received by the editor at least one month in advance. It is often impossible for the editor, because of limited time and personnel, to acknowledge individually all material received.

CIRCULATION POLICY

The Newsletter is distributed, without charge, to interested military and government agencies, to contractors for the Federal Government, and to contributors of material for publication.

For many years, in addition to the ONR initial distribution, the Newsletter was reprinted by the Association for Computing Machinery as a supplement to their Journal and, more recently, as a supplement to their Commun' ations. The Association decided that their Communications could better serve its members by concentrating on ACM editorial material. Accordingly, effective with the combined January-April 1961 issue, the Newsletter became available only by direct distribution from the Office of Naval Research.

Requests to receive the Newsletter regularly should be submitted to the editor. Contractors of the Federal Government should reference applicable contracts in their requests.

All communications pertaining to the Newsletter should be addressed to:

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COMPUTERS AND DATA PROCESSORS, NORTH AMERICA

ADVANCE II, ASI-420 AND ASI-210— ADVANCED SCIENTIFIC INSTRUMENTS, INC., MINNEAPOLIS 22, MINNESOTA

Advanced Scientific Instruments, Inc., has designed three computers which cover the field in computing and data processing capability. They are, in order of decreasing size, the ADVANCE II, the ASI-420, and the ASI-210

All three machines are high speed, parallel, internally programmed, solid-state

computers with random access core memories having a total cycle time of 2 microseconds, including addressing of the next word. All of the computers have extensive input-output buffering facilities which make them adaptable to real-time applications, and which permit the integration of large quantities of peripheral equipment.

To date ASI has delivered one 210 to Goddard Space Flight Center, one 210W (a modified 210) to Argonne National Laboratory, and has announced the sale of another to Chance Vought Corporation.

The 210 system sold to Chance Vought carries a price tag of $113,000. The medium scale ASI-420 sells for $324,000, and the larger scale ADVANCE II for $860,000.

Programming

The instructions used in all ASI computers are divided into two classes, termed class A and class B. Class A instructions are used universally in all three machines, and programs prepared with class A instructions can be executed on any ASI machine. Class B instructions are used only with the larger ASI-420 and ADVANCE II computers; programs prepared with the class B instructions can be executed without modification only on the larger machines.

Input-Output

The input-output system of the ADVANCE II computer consists of several input-output assembly registers and an independent control system. Information can be exchanged between the computer and external devices completely independently of arithmetic operations, and the input-output system can provide off-line communications between items of peripheral equipment. The total information transfer rate of the ADVANCE II input-output system is 250,000 words per second. Additionally, the ADVANCE II has a direct, high speed input-output channel capable of 500,000 42-bit word transfers per second.

The ASI-420 and ASI-210 computers also use input-output assembly registers for external communication, but these are controlled by the central control system. The transfer of a block of information is initiated with a single instruction. Thereafter, each assembly register is serviced by the memory during specific times set aside for this purpose in all instructions, and the program is not further affected by the transfer. In other words, the memory is time shared by the arithmetic and input-output sections of the computer.

Either fixed or variable block transfers are made possible by two memory address registers associated with each assembly register. One of these registers contains the address of the first word of the block, and the other contains the address of the last word of the block. With the transfer of each word, the first register is incremented. When the contents of the registers are identical, the block has been transferred and input-output operation ceases. The size block can be varied simply by the addresses entered originally into the address registers.

Advance II

The ADVANCE II computer is a 42-bit machine with a memory expandable to 32,768 words. The computer has an optional maximum of eight buffered input-output channels with a combined transfer rate of 250,000 words per second. Arithmetic speeds of the computer are:

Operation	Speed (μsec)
add	6
multiply	33
divide	33

The speed of the machine is enhanced by an instruction look-ahead feature in which the next instruction of a program is extracted from the memory, and indexing of the operand is performed while the current instruction is being executed. This operation is performed simultaneously with arithmetic operations because the memory address register is not used in arithmetic functions, and the indexing addition is performed in an independent 15-bit adder. When the current instruction is completed, the next instruction is immediately ready.

An 84-bit, 512-word magnetic core memory stores micro-program commands from which the instructions of the computer are constructed. The operation code of an instruction is translated to the address of the first command in the micro-program memory. Thereafter, the memory is stepped through successive memory locations, and the resultant commands complete the instruction. Any command or sequence of commands can be repeated under control of a repeat counter.

The micro-program memory can be filled or replaced from either the main memory or the paper tape reader of the computer. Instruction substitutions can be made easily, and unique instructions for specific applications can be formulated from the available micro-commands. This feature provides the ADVANCE II with exceptional flexibility.

One of the most powerful features of the ADVANCE II is its ability to communicate with other ASI computers in multi-computer complexes. Such communication can be effected both through the real-time, high-speed, input-output channels and through the buffered channels. Each computer regards the other merely as external devices, and through the facilities of the trapped interrupt, can be alternately isolated from the other computers or enabled to participate, all under program control. In this way, "executive privilege" for one computer is not necessary, and independent computer programs can be "merged" effectively. Inter-computer communication is made possible simply by wiring, and no auxiliary electronics is required.

ASI-420

The ASI-420 is a 42-bit machine with a memory expandable to 16,384 words. The computer has an optional maximum of six input-output buffer channels with a combined transfer rate of 125,000 words per second. Arithmetic speeds of the machine are:

Operation	Speed (μsec)
add	10
multiply	64
divide	98

The speed of the ASI-420 is less than that of the ADVANCE II because of the time allowed in each instruction to service the input-output buffer registers. This time is allowed whether or not input-output data is transferred, and remains the same regardless of the number of channels used. Therefore, the transfer rate of 125,000 words per second is constant for machines with any number of buffer channels.

ASI-210

The ASI-210 is a general purpose, high speed, solid-state digital computer of small size. It is well suited to applications in scientific and engineering computations, data reduction, and real-time process control. The ASI-210 has the following outstanding features:

1. Stored program, parallel operation, solid-state circuits, 21-bit word length, and magnetic core memory expandable to 8192 words.

2. Buffered input-output channels with total transfer rate of 62,500 21-bit words per second. Number of buffered channels is one, with one additional channel optional. Buffers can be used in an effective manner off-line for conversion operations.

3. Multiple indexing using index words stored in the computer memory.

4. Indirect addressing. Successive indirect addressing is possible with indexing at each step.

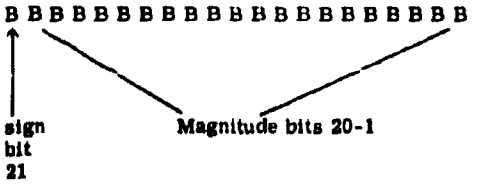
5. Trapped interrupt. Logic circuits, which sense interrupt events, can be armed or disarmed under program control to jump the program into corresponding sub-routines upon occurrence of the event. The trapped interrupt feature saves a great deal of time and memory in programs because the interrupt conditions do not have to be tested repeatedly. It is also useful in cases where two or more computers are used together in the same system, or where a computer converses with several items of peripheral equipment.

6. One-megacycle phase rate operation. Add time 10 microseconds; multiply time 54 microseconds, including indexing and memory access time.

7. Six sense switches. Program branching may be controlled by sense switches on the operators console.

8. No air conditioning is required. High reliability operation in extreme temperature and humidity conditions. Equipment is designed to operate in ambient 32° to 125°F at 95 percent relative humidity.

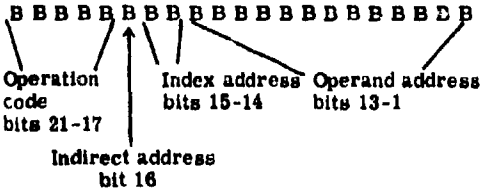
Number Format



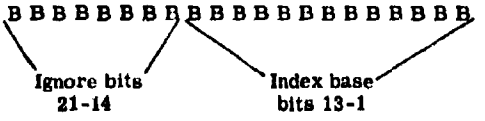
B represents 1 binary digit.

INSTRUCTION FORMAT

Instruction Word



Index Word



B represents 1 binary digit.

Instruction List

Notation

A	Register A is the accumulator
E	Register E is a second major arithmetic register
( )	Contents of, for example, (A) signifies the contents of the A register
+	Add
-	Subtract
.	Multiply
÷	Divide
⟶	"is placed in"
| |	Absolute value, for example, (A) signifies the absolute value of the contents of the A register
‾‾	Complement of, for example, ($\bar{A}$) signifies the complement of the contents of the A register
⊕	Logical OR, for example, ($\bar{E}$) ⊕ (m) signifies the logical OR of the complement of the contents of the E register and the operand
⊙	Logical AND, for example, (E) ⊙ (m) signifies the logical AND of the contents of the E register and the operand
a	Register A designator in the operand address
e	Register E designator in the operand address
s	Shift right designator
c	Shift circular designator
g	Gray to binary shift indicator
k	Shift count
i_b	Index base
p	Effective operand address
m	The memory location specified by p
i	Address of present instruction
(m)	Operand

Unless otherwise indicated, the operand address is subject to indexing and indirect address.

Arithmetic

The adder used in the ASI-210 is a closed loop binary adder using left end-around carry operation in the one's complement addition. The sign bit (21) is a zero (0) for positive numbers and a one (1) for negative numbers. This is useful in most operations using the entire register A. However, in certain instances such as indexing, only a small portion of the adder is used and provisions to prevent end-around carry are made. Operation is then carried out

in the two's complement addition which gives the correct answer without carry. A comparison of the two systems is shown:

Decimal	Binary	1's Comp.	2's Comp.
3	011	+3	+3
2	010	+2	+2
1	001	+1	+1
0	000	+0	+0
7	111	-0[a]	-1
6	110	-1	-2
5	101	-2	-3
4	100	-3	-4

[a] -0 is meaningless. All carries are forcibly entered in adder so that the number becomes 000 or +0.

ASI-210 Instruction Chart

Octal Code	Instruction	Including Index & I/O Time (μsec)	Not Including Index & I/O Time (μsec)
00	HALT	8	
02	JUMP	8	4
04	RETURN	12	8
06	END INTERRUPT	8	4
10	ADD	10	6
12	SUBTRACT	10	6
14	LOAD A	10	6
16	LOAD E	12	8
20	ABSOLUTE VALUE	8	4
22	NEGATE	8	4
24	CLEAR	12	8
26	STORE A	8	6
30	MULTIPLY	54	50
32	DIVIDE	56	52
34	ROUND	14	10
36	STORE A ADDRESS	10	6
40	COMPARE < A	14	10
42	COMPARE = A	14	10
44	TEST A < 0	10	6
46	STORE E	10	6
50	AUGMENT INDEX	12	12
52	TEST INDEX	10	10
54	STORE ADDRESS	12	12
56	LOGICAL OR	12	10
60	SHIFT	10+2K	6+2K
62	NORMALIZE A	14+2K	10+2K
64	NORMALIZE A,E	14+2K	10+2K
66	LOGICAL AND	12	10
70	TRAP	8	4
72	SENSE SWITCH	10	6
74	EXTERNAL DEVICE	16	12
76	ASSEMBLY REGISTER	20	16

Explanation of Instructions

10 ADD (A) + (m) → A

Add the operand to (A). The sum will appear in Register A. This instruction can result in an add overflow.

12 SUBTRACT (A) - (m) → A

Subtract the operand from the contents of A. The difference will appear in Register A. This instruction can result in an add overflow.

30 MULTIPLY (A) · (m) → AE

Multiply the contents of A by the operand. The most significant bits of the product will appear in Register A and the least significant bits in Register E.

32 DIVIDE (AE) ÷ (m) → E rem → A

Divide the contents of A and E by the operand. The quotient will appear in Register E and the remainder in Register A. A fault interrupt may occur if the contents of A is greater than or equal to the operand.

24 CLEAR 0 → A, or 0 → E, or 0 → AE

Clear A if the a designator bit 12 of the operand address is a 1. Clear E if the e designator bit 11 of the operand address is a 1. Clear A and E if the a and e designator bits 12, 11 of the operand address are 1's.

22 NEGATE $(\bar{A}) \rightarrow A$, or $(\bar{E}) \rightarrow E$, or $(\bar{AE}) \rightarrow AE$

Complement the contents of Register A if the a designator bit 12 of the operand address is a 1. Complement the contents of Register E if the e designator bit 11 of the operand address is a 1. Complement the contents of Register A and E if the a and e designator bits 12, 11 of the operand address are 1's.

20 ABSOLUTE VALUE $|(A)| \rightarrow A$, or $|(E)| \rightarrow E$, or $|(AE)| \rightarrow AE$

Make the contents of A positive if the a designator bit 12 of the operand address is a 1. Make the contents of E positive if the e designator bit 11 of the operand address is a 1. Make the contents of A and E positive if the a and e designator bits 12, 11 of the operand address are 1's.

34 ROUND (E20) + (A) → A

Add the most significant bit of Register E to the contents of A in the least significant bit. The result will appear in Register A. Register E will be unchanged.

36 STORE A ADDRESS $(A_{13-1}) \rightarrow (m_{13-1})$

Stores operand address portion of (A) in the operand address portion of the operand (m).

Transfer

14 LOAD A (m) → A

Bring the operand to Register A.

16 LOAD E (m) → E

Bring the operand to Register E.

26 STORE A (A)⟶m

Store the contents of A in the memory location specified by the operand address.

46 STORE E (E)⟶m

Store the contents of E in the memory location specified by the operand address.

60 SHIFT

Bit Designator	12 a	11 e	10 s	9 c	8 g	7-1 k
SHIFT (A) RIGHT	x		x			x
SHIFT (A) LEFT	x					x
SHIFT (A) LEFT CIRCULAR	x			x		x
SHIFT (E) RIGHT		x	x			x
SHIFT (E) LEFT		x				x
SHIFT (E) LEFT CIRCULAR		x		x		x
SHIFT (AE) RIGHT	x	x	x			x
SHIFT (AE) LEFT	x	x				x
SHIFT (AE, LEFT CIRCULAR	x	x		x		x
CONVERT (E) FROM GRAY CODE TO BINARY LEAVING THE RESULT IN A					x	x

See "INSTRUCTION LIST, Notation" for definition of designators a through k.

Right shifts are open-ended shifts. Left shift may be either open-ended or circular shifts. In open-ended shifts, the bits introduced into the register are identical to the sign bit 21 which remains unchanged. In circular shifts, the sign bit 21 is shifted along with the number. The number of shifts, specified by the shift count (k), cannot exceed 63 decimal (2^6-1).

62 NORMALIZE A (A) · 2^k until A20 ≠ A21, and, k + (m)⟶m

Shift the contents of A left, leaving the sign bit 21 unchanged, until the sign bit 21 and the most significant bit 20 are different. With each shift, the sign bit will be entered in the least significant bit 1 of A and the most significant bit 20 of A will be lost. Add the number of shifts required to the operand address portion of the operand specified by the operand address.

64 NORMALIZE A AND E (AE) · 2^k until A20 ≠ A21, and, k + (m)⟶m

Shift the contents of A and E left, leaving the sign bit 21 unchanged, until the sign bit 21 and the most significant bit 20 of A are different. With each shift, the sign bit 21 of E will be entered in the least significant bit 1 of E, and the most significant bit 20 of E will be entered into the least significant bit 1 of A. The most significant bit 20 of A will be lost. Add the number of shifts required to the operand address portion of the operand specified by the operand address.

66 LOGICAL AND (E)⊙(m)⟶A

Form the logical "and" of the operand and the contents of E in Register A. An example of the bit-for-bit result is as follows:

Contents of E	1100
Operand	1010
Logical and	1000

56 LOGICAL OR (E) ⊕ (m)⟶A.

Form the logical "or" of the operand and the contents of E in Register A. An example of the bit-for-bit result is as follows:

Contents of E	1100
Operand	1010
Logical or	1110

50 AUGMENT INDEX $p + I_b \longrightarrow I_b$

Add the specified operand address to the index base, and replace the index base with the sum. This instruction can result in an index overflow. The addition will be in the two's complement system. This instruction permits decrementing as well as incrementing.

52 SKIP IF INDEX HIGH

The specified operand address of this instruction is the complement of the index limit address. This limit address is in one's complement if the limit is positive, and in two's complement if the limit is negative. When the index base (contents of the index register in two's complement format) exceeds the limit address, the next instruction in sequence will be skipped. . .otherwise the instructions will continue in sequence. The skip will occur when the addition of the 13-bit limit address with the 13-bit index base causes a carry into the 14th bit position.

Examples

If the index base exceeds four and it is desired to skip, the index limit address will be:

1 1 1 1 1 1 1 1 1 1 0 1 1 (Binary - one's complement)

	14th Bit		14th Bit	
Index Base	X	0 0 0 0 0 0 0 0 0 0 1 0 0	X	0 0 0 0 0 0 0 0 0 0 1 0 1
Index Limit	X	1 1 1 1 1 1 1 1 1 0 1 1	X	1 1 1 1 1 1 1 1 1 0 1 1
Sum	X	1 1 1 1 1 1 1 1 1 1 1 1 1	1	0 0 0 0 0 0 0 0 0 0 0 0 0
	No skip occurs when index base = 4		Skip occurs when index base = 5	

If the index base exceeds -4 and it is desired to skip, the index limit address will be:

0 0 0 0 0 0 0 0 0 0 0 1 1 (Binary - two's complement)

	14th Bit		14th Bit	
Index Base	X	1 1 1 1 1 1 1 1 1 1 1 0 0	X	1 1 1 1 1 1 1 1 1 1 1 0 1
Index Limit	X	0 0 0 0 0 0 0 0 0 0 1 1	X	0 0 0 0 0 0 0 0 0 0 1 1
Sum	X	1 1 1 1 1 1 1 1 1 1 1 1 1	1	0 0 0 0 0 0 0 0 0 0 0 0 0
	No skip occurs when index base = -4 (in two's complement)		Skip occurs when index base = -3 (in two's complement)	

(i.e., if the limit desired is a negative number, the rule is the following:

|limit| -1 = index limit address)

04 RETURN $i + 2 \rightarrow m_{1 \text{ thru } 13}$

Store the address of the instruction following the next sequential instruction in the operand address of the operand. By letting the operand be a jump instruction at the end of a sub-routine, the program can jump into the subroutine on the next instruction and return to its program sequence at the end of the sub-routine.

02 JUMP

Take (m) as the next instruction.

00 HALT

Halt, and take (m) as the next instruction when operation is resumed.

40 COMPARE < A $(m) < (A)$, skip and take $i + 2$
$(m) \geq (A)$, take $i + 1$

If the operand is less than the contents of A, skip the next instruction of the sequence.

42 COMPARE = A $(m) = (A)$, skip and take $i + 2$
$(m) \neq (A)$, take $i + 1$

If the operand equals the contents of A, skip the next instruction of the sequence.

44 TEST A < 0

If (A) are less than 0, take next instruction from operand.

54 STORE ADDRESS IN INDEX $p \rightarrow I_b$

Store the operand address in the base address portion of the memory location specified by the index address. The operand address will not be indexed.

06 END INTERRRUPT

Take (m) as the next instruction, then discontinue the interrupt. This instruction must be used at the end of an interrupt routine.

70 TRAP

If bit 12 of the operand address is a "1," the contents of the trap flip-flops will be stored in operand address portion of register A in the bit positions specified below. If bit 11 is a "1," the specified traps will be armed. If bit 10 is a "1," the specified traps will be disarmed. If bit 13 is a "1," the contents of the Add overflow and Index overflow flip-flops may be stored in the bits of A corresponding to their trap designators. These two flip-flops will be reset by recognition of interrupt or by storage in A as described. Bit specification of the operand address of the Set Trap instruction:

13 Store flip-flop designator
12 Store trap designator
11 Arm trap designator
10 Disarm trap designator
1 External device interrupt trap
2 Busy interrupt trap
3 Operator interrupt trap
4 Fault interrupt trap
5 Add overflow interrupt trap
7 Index overflow interrupt trap
8 Operator control light 1
9 Operator control light 2

74 EXTERNAL DEVICE

Interpret the operand as an external device control word (EDCW). A busy interrupt could result from this instruction. The external device control word is described in detail under external device instruction.

72 SENSE SWITCH

If any of the sense switches 1-6 specified in the operand address bits 1-6 is set, skip the next instruction in the normal sequence. If the next instruction is a jump instruction, this is in effect a programmed jump that is conditional upon the sense switches. These switches may be changed at any time by the operator. If more than one sense switch is specified, the skip will occur if any of the specified switches is set.

76 ASSEMBLY REGISTER

Interpret the operand as an assembly register control word (ARCW). A busy interrupt can result from this instruction. The assembly register control word is described in detail under assembly register instruction.

Trapped Interrupt

A number of events can cause the program of the computer to be interrupted. Some of these are:

Busy	Operator
Add Overflow	External device
Fault	Index overflow

An interrupt trap associated with each event may be set under program control to either respond when the event occurs or to ignore it. The traps are controlled by the "trap" instruction. Bits 11 and 10 in the operand address designate whether the specified traps will be armed or disarmed, and bits 9 through 1 of the operand address specify which traps (or indicator flip-flops) are to be armed (set) or disarmed (cleared). If bit 12 of the operand address is present the condition of each of the traps will be stored in the operand address portion of register A in the bit position that corresponds to the designating bit for that particular trap in the "trap" instruction. This will occur before any changes are made in these conditions as a result of bit 11 or 10 occurring in the same "trap" instruction. This is very useful in sub-routines that require the use of these traps, but that also must return these traps to their previous condition at the end of the sub-routine.

By specifying bit 13 in the trap instruction, the contents of the Add overflow and Index overflow flip-flops may be stored in the bits of A corresponding to their trap designators. These three flip-flops will be reset by recognition of interrupt or by storage in A as described.

If a particular trap is set to respond to the occurrence of an event, an interrupt is initiated when the event occurs (and the interrupt routine flip-flop is set). As a result of this interrupt, the current instruction will be completed and the address of the following instruction will be stored in the interrupt fixed address (00110). Then control is transferred to a unique fixed address (identified below) associated with the particular event or condition which caused the interrupt. The contents of the unique fixed address will usually be a jump instruction leading to a sub-routine. Thus, the programmer may have a different sub-routine for each event that may cause an interrupt. The sub-routines will be entered without the necessity of the programmer writing a decoding program to find which sub-routine to enter since the occurrence of a particular interrupt causes a jump to a particular sub-routine. At the end of each sub-routine is a jump to the interrupt fixed address (00110). In the interrupt fixed address is an "end interrupt" instruction which is identical to a jump instruction except that it clears the interrupt routine flip-flop. The "end interrupt" instruction will cause a return to the main program at the point where it was interrupted. Only a priority external device may interrupt an "interrupt sub-routine." When automatic interrupts are not available, the programmer must write a scanning program that repeatedly checks certain conditions to see whether the main program should be interrupted. The ability to use the trapped interrupt feature to handle such conditions as arithmetic overflow gives the programmer the opportunity to make any necessary corrections and reenter the main program to continue the calculations. By being able to selectively arm and disarm traps, the programmer has complete program control over either initiating an interrupt when a particular condition occurs or ignoring its occurrence.

The following is a description of the interrupt conditions:

BUSY interrupt will occur if an external device is instructed to do something which it cannot do because either the device or its assembly register is busy. This interrupt may also occur if an "assembly register" instruction addresses a busy channel.

External Device Interrupt

External device interrupt will occur when an ED sends a signal to the central computer that it desires to transmit information. External device interrupt addresses are assigned octal numbers from 00000-00077. These numbers are scanned through periodically to see if an ED requests interrupt. The normal ED's are assigned interrupt addresses at the low end of the memory (i.e., 00,02,04,06, ...) corresponding to the ED addresses. When an ED requests interrupt, the ED interrupt flip-flop is set, the current instruction is completed and the address of the next instruction is stored in a fixed location 00110. Then control is transferred (jumped) to the interrupt address corresponding to the ED address which requested the interrupt. An "end interrupt" instruction, which is identical to a jump instruction except that it clears the interrupt sub-routine flip-flop, may be inserted in the interrupt fixed address. Certain ED are assigned priority interrupt addresses in a block at the higher end of the memory (i.e., ...,66,68,70,72,74,76). The lowest number in the block has the highest priority. Only these priority interrupt devices can interrupt a "normal interrupt sub-routine." If a priority ED requests interrupt, the scanner jumps to the priority block and scans through for the highest priority ED requesting interrupt. A second flip-flop is set, the next instruction is stored in fixed location 00114 and control is transferred to priority ED. When the priority interrupt sub-routine is completed and an "end interrupt" jump is executed, the priority interrupt flip-flop alone is reset. The normal interrupt

flip-flop is maintained in its set condition. After the interrupt is recognized, the scanner will look for any other priority interrupt. If none is requested, control may be transferred to the original interrupt sub-routine. After this sub-routine is completed and an "end interrupt" jump is executed, the first flip-flop is reset and control may be transferred to the main program.

External devices in which a failure is of critical interest to the running program are assigned a second number (normally the odd address following the proper ED address; i.e., 01,03,05,...). This address is not employed in any ED instruction, but is the address of the fixed memory location associated with a failure interrupt by the particular ED. Thus, there is the possibility of two interrupt routines associated with a particular ED: one for normal interrupt and one for failure.

Fault Interrupt

Fault interrupt will occur for the following reason:

Dividend $\geq$ divisor in "divide"

Add Overflow Interrupt

Add overflow interrupt will occur when the result of addition or subtraction exceeds the length of the arithmetic register and changes the sign bit 21.

Index Overflow Interrupt

Index overflow interrupt will occur when the result of the augment index instruction exceeds the length of a memory address.

Memory Fixed Addresses

Octal	
00000-00077	External device interrupts
00100	Operator interrupt
00101	Unspecified
00102	Fault interrupt
00103	Add overflow interrupt
00104	Exponent overflow interrupt
00105	Index overflow interrupt
00106	Busy interrupt
00107	Unspecified
00110	Interrupt fixed address
00114	Priority ED interrupt fixed address
00115-00117	Index registers

Input-Output System—General Features

All transfer of data to or from the computer is conducted via input-output channels which communicate directly with the magnetic core memory of the ASI-210. The access to the memory is time-shared between the operating program and input-output data transfer; in a typical situation, approximately 15 percent of the memory time is available for input-output data transfer. Since the arithmetic and control functions of the operating program do not require access to the memory every computer cycle, they may proceed simultaneously with input-output data transfer with little or no loss in speed.

The standard ASI-210 is provided with one input-output channel. An additional channel may be optionally supplied.

Each piece of on-line peripheral equipment is known as an "External Device" (abbreviated, E.D.). Each external device has an unique address. The ASI-210 can accommodate up to 64 external devices with two-channel operation.

The ASI-210 input-output system is provided with program interrupt features so that testing of the condition of the external devices by the running program is not necessary.

MULTIPLE-PROCESSOR G-21— BENDIX COMPUTER DIVISION, LOS ANGELES, CALIFORNIA

Bendix Computer Division is developing a large-scale special purpose computer system with a vast memory and true parallel processing capabilities. The super-system, designated the G-21, will be a multiple-processor computer using proven off-the-shelf components of the G-20 computer system. It will be capable of handling massive amounts of data fed to it from a variety of sources on an on-line, real-time basis.

The system is designed for special military control applications which require the collecting and processing of large amounts of intelligence and operational data for immediate presentation to military commanders.

Large Memory

The key to the new G-21 system is the multiple processor design which affords one of the largest memory reservoirs. Up to three

central processor units (CPU's), with 57,344 words of random access common core memory, can be linked in a single system. An additional 8192 words of exclusive memory is reserved for each processor, thereby giving a total high-speed memory capacity of 81,920 words.

Three segments of the same problem or three separate problems may be handled simultaneously with this configuration.

If necessary, several G-21 systems may be interconnected without modification of existing equipment. Transfer of data between systems at extremely high speeds will be possible through completely buffered communication lines under the control of independent input-output processors.

Input to the G-21 in a complex military control center, could come from any number of sources, such as, radar, teletype, microwave, telephone, A/D converters, and analog and digital computers, as well as from conventional computer input units.

24-Hour Problems

Unusual flexibility of the G-21 would allow it to handle so-called "24-hour problems" – continuously receiving data from a number of sources, processing the data, and finally delivering outputs in a variety of forms ranging from luminescent screen display to teletype signal, or even to the firing of a weapon. Design of the system also allows individual problems to be handled without interrupting the 24-hour operation.

A unique self-adapting feature is built into the machine's programming. An executive control program, designed to meet specific user requirements, would recognize the demands being placed on the system, and assign appropriate processors to the same sequence of operations stored in one portion of the common memory, or it can assign one processor to a sequence of operations without affecting the activities of the other processors. It also will switch the role of a processor, at will, among many functions.

True Parallel Processing

This flexibility affords true parallel processing, eliminating the need for parts of a programming system to operate sequentially. Information can now be traded instantly through use of data tables common to the multiple processors. Through program modules, operating simultaneously, reaction time of one module to conditions as they are identified by another is reduced significantly.

A "fail-safe" feature of the executive program will insure system reliability. If one of the processors should fail, the remaining processors will automatically adjust and hold lower-priority problems until time is available. The most important problems assigned to the machine would be unaffected.

Field tests of G-21 components already in use at G-20 installations indicate assured high-reliability standards for the new machine. As an example, figures gathered from the early months of customer use of the central processors units show an availability record of better than 99 percent.

G-21 Programs

Programming packages for the G-21 will include many of the compilers, assemblers, routines, and sub-routines developed over the past 3 years for the G-20.

The G-21 is the second phase in the development of a universal computer design aimed at eliminating the obsolescence problem for computer users. Future Bendix computer developments will be keyed to G-20 and G-21 concepts, to provide compatibility with existing systems.

Standard hardware elements, in addition to the central processors, include high-speed magnetic tape units, high-speed printers, disc memory units, auxiliary core memory units, control buffers, data communicators, and punched-card and punched-paper tape units.

Price of the system will vary according to application needs, but a minimum G-21 system (two CPU's, one data communicator, three memory units, one high-speed line printer, three magnetic tape units) will cost upwards of $1,250,000. Approximate delivery date will be 18 months from receipt of order.

CONTROL DATA 3600—
CONTROL DATA CORPORATION, MINNEAPOLIS 20, MINNESOTA

Control Data Corporation recently released details on their new, powerful, large-scale digital computer - Control Data 3600. This computer features modular expandability of its high-speed magnetic core memory, high-speed data communication channels, and computing power. Control Data Corporation takes pride in making this announcement less than 2-1/2 years after delivery of their first large-scale computer - the highly successful 1604. The first 3600, with a complete programming system included, is scheduled to be ready for delivery in approximately 1 year.

The system is exceptionally suited for handling large-volume data processing and solving large-scale scientific problems at very high speeds. The advanced level of speed and flexibility in the 3600 are especially important in real-time applications where computed results must be available nearly as fast as the problem is presented to the computer. The special features in the 3600 offer superior inherent machine capabilities at a price substantially less than other computers approaching the capabilities of the 3600. One of these advanced capabilities is the modular design of the 3600 which permits smooth expansion of a basic 3600 system in step with the user's increased requirements as they arise. This is achieved without the necessity of inter-connecting the modules with control units, or "black boxes."

The magnetic core memory of the 3600, expandable in modules from 1-1/2 million bits of information to more than 12-1/2 million bits, has an information access time of less than 1 microsecond. The 3600 utilizes special circuits, which make use of tunnel diodes, to speed up basic arithmetic processes in the nanosecond (or billionths of a second) range.

In transmitting data to and from peripheral equipment, the data communication module operates independently and asynchronously of the main computer program. Each data communication module has four bi-directional data channels, expandable to eight at the customer's option. These high-speed channels permit data to be transmitted to and accepted from peripheral equipment in large-volume and at tremendously high speeds while the computer continues to perform highly complex computations. As many as 32 bi-directional data channels can be incorporated in the fully expanded 3600, each able to handle up to eight control and/or peripheral devices.

A complete programming system will be delivered with the first 3600 computer system. Oriented around the Control Data Master Control System (MCS), the computer programming will be totally independent of the hardware-size and type of a given 3600 system, whether the customer has a basic or an expanded version. Therefore, the programming will be as tailor-made to the customer's requirements as is the hardware used. The MCS provides for a common library to incorporate systems programming such as FORTRAN and COBOL, an open-ended feature to incorporate new compilers and programming systems as they are developed, and a "linking-loader" feature to incorporate several independently compiled or assembled sub-programs into one main computer program.

A basic 3600 computer system, including necessary peripheral equipment, is in a purchase price range of $2 to $2-1/2 million. Lease of the same equipment will be approximately $55,000 to $60,000 per month. This price includes, as standard 3600 computer hardware, many features that are generally held as optional in other systems approaching the capabilities of the 3600. For example, both fixed- and floating-point arithmetic, in both single and double precision, is standard in all 3600 systems.

Characteristics

Modular Design and Expandability

Basic System	Expandable to
3604 Compute Module	As many as five compute modules can be linked together.
3603 Storage Module 32,768 48-bit words in each module, each word with 3 parity bits	Expandable in 32,768-word modules to a total of eight for more than 12-1/2 million bits of information.
3602 Communication Module Equipped with four (4) high-speed 3606 Data Channels	Expandable up to eight data channels per module, up to eight modules per 3600 computer. Total expansion to 32 bi-directional channels. (As many as eight control and/or peripheral devices can be handled by each bi-directional data channel.)
3601 Console Includes input-output electric typewriter	
250-card-per-minute punched card reader	

Operating Speeds

Magnetic Core Memory

Memory cycle time---------- 1.5 microseconds

Effective cycle time (access) ---------- 0.7 microseconds

Internal Computing Speeds

Typical average execution times are given in microseconds.

Instructions	Fixed Point	Single Precision Floating Point	Double Precision Floating Point
Multiply	1-6	1-6	2-26
Divide	1-14	1-14	2-26
Fetch/Store	1.5-2.2	1.5-2.2	3
Add/Subtract	1.5-2.2	4	5

Special High-Speed Circuits

These special circuits employ tunnel diodes to speed up basic arithmetic operations into the nanosecond range. These operate at 4 nanoseconds per stage.

The basic cycle time of the adder network, for example, is 250 nanoseconds. The shift time is a constant 250 nanoseconds regardless of the number of places shifted.

Examples of Arithmetic Function Speeds

The 3600 Computer can perform the following functions in 1 second:

670,000 fixed-point additions or subtractions

250,000 floating-point additions or subtractions in single precision

200,000 floating-point additions or subtractions in double precision

167,000 floating-point multiplications (single precision)

71,500 floating-point divisions (double precision)

38,500 floating-point multiplications and/or divisions in double precision

Input-Output Communications

Input and output operations occur independently and asynchronously with operations in the compute module. The standard four bi-directional data channels in each communication module (or expanded modules with eight channels) permit data to be transmitted to and accepted from peripheral equipment in large volume and at tremendously high speeds while the computer continues to perform highly complex computations. The computer only directs the selection of a specific external device and the channel in which the I/O activity is to take place. Once operating conditions have been initiated, the communication module supervises all I/O functions. Data being transmitted or received goes to or from the magnetic core memory directly, and does not pass through the compute module.

Computation Capabilities

The 3604 compute module performs all computing and logical operations in the 3600 system. Included as standard hardware in the compute module are provisions for fixed- and floating-point arithmetic in both single and double precision. The 3604 operates in a parallel binary mode.

Several new categories of instructions have been included in the 3600 instruction repertoire:

1. Commands for manipulating portions, or "bytes," of a data word. For example, bytes of 48 bits or less may be transmitted to any portion of a computer register or memory storage word in a single operation. Indexing through bytes in a word (horizontally) or through a list of such words (vertically) in the same operation is also provided.

2. Double-precision, floating-point commands include add, subtract, multiply, divide, fetch, and store. (A 10-bit plus sign exponent is used with an 84-bit plus sign fraction.)

3. A special instruction for list processing, as well as several new indexing operations.

4. A universal bit-sensing instruction that permits any bit to be tested and branched upon.

5. A powerful, extremely fast, interrupt facility is provided, as well as instructions for processing interrupts.

6. Six sense switches are included on the console and can be programmed sensed. These are in addition to three selective jump and three selective stop switches.

7. A 48-bit sense-light register able to set or clear each position in a register under program or manual control.

8. Two bounds registers of 18 bits each, used for memory lockout. Information is not written into the region of the memory specified by the addresses within the bounds registers.

Other important features in the 3600 are:

1. Two-way search instructions

2. Auto-load buttons for card and magnetic tape equipment

3. Direct card reader entry into arithmetic register

4. Parity check on all I/O data transmission

5. Special computing functions can be added easily via special channel in the compute module (i.e., trigonometric and exponential functions, etc.).

Programming

In parallel with the development of the 3600, Control Data is developing a complete and integrated software system to be delivered with the first computer. This software system will be oriented around a Master Control System (MCS).

The MCS will act as a common communication link among all programming systems and I/O devices, interrupt, and memory allocation functions. Thus, the MCS will allow programming systems to be independent of particular machine configurations, as well as of types and numbers of I/O media. In addition, the MCS will provide:

1. A library common to all systems, such as FORTRAN and COBOL, which will operate within the MCS.

2. An open-ended ability to incorporate new compilers and operating systems as they are developed.

3. A linking loader that will permit joining together, in one program, several sub-programs that may have been separately and independently compiled or assembled.

4. A system easy to modify and adapt, when necessary, to the needs peculiar to a given installation.

Some of the important programming systems operating under control of the MCS will be:

MONITOR SYSTEM. A complete operations supervisory system for automatic control of all jobs. It will allow stacking of jobs with arbitrary intermixing of different job types, such as assembly, compilation, and execution.

COMPASS. A comprehensive assembly system with versatile language features for representing the extensive instruction repertoire in a simple symbolic notation, employing advanced assembly techniques.

FORTRAN. An algebraic compiler with extensions to, and generalizations of, the basic FORTRAN language using advanced compiler techniques for producing optimum object programs.

COBOL. A complete compiling system for business-oriented applications.

1604 Compatibility Package. A software package which will execute interpretively all trapped I/O instructions of a 1604 program running in the 1604 compatibility mode.

Optional Peripheral Items

A variety of optional on/off-line peripheral items may be used with the 3600 computer. These include 12-, 24-, and 48-bit bi-directional data channels; a 48-bit inter-computer data channel; special function generators; magnetic tape handlers and tape synchronizers; medium- and high-speed card readers, card punches; low- and high-speed line printers; paper tape I/O equipment; keyboard entry devices and typewriters; and disc files.

CONTROL DATA 6600—
CONTROL DATA CORPORATION,
MINNEAPOLIS 20, MINNESOTA

Control Data Corporation has announced that the Company has received from the U.S. Atomic Energy Commission a $5,574,000 order to furnish and install a super, high-speed computer system at the Lawrence Radiation Laboratory. The system, called the Control Data 6600, is to be installed and ready for acceptance testing at the Livermore (California) laboratory not later than February 29, 1964. The Lawrence Radiation Laboratory is operated for AEC by the University of California.

Control Data Corporation was selected to furnish the new system on the basis of its proposal made in response to a solicitation to the computer industry by AEC in 1961, with the delivery of the system requested in mid-1963. Under the terms of the negotiated contract, the Company will furnish interim computer capacity on the Control Data 3600 Computer System (see 3600 description, this issue of DCN) until the new system is accepted. The request for proposals stipulated that the system required, although faster than any existing machine, was not to be a specially designed

computer. It was to be capable of high speed operation for employment in the solution of broad complex scientific problems.

The Control Data 6600 Computer System includes a single central processor with a high-speed arithmetic and logical unit, a central memory of 61,440 words, peripheral processors, associated consoles, and input-output equipment. The system central processor is a high-speed, logical and arithmetic unit, especially designed for rapid floating-point operations.

The high speed in computing is obtained through the use of semi-micro instructions and multiple transistor registers for temporary storage. Simple instructions can be combined optimally to execute complicated sequences without loss of time in referencing core storage temporary locations.

The new computer system will enable scientists to cope with the increasingly complex problems that scientific advances pose and to obtain solutions to present problems in finer overall detail. The new system, which was designed to be faster than any now existing, will make it possible to solve in shorter time comprehensive technical problems that now require many hours of machine operation. Thus, the addition of CONTROL DATA 6600 will significantly increase the overall work capacity of the Lawrence Radiation Laboratory.

HYDAC SERIES 2000—HYBRID DIGITAL/ ANALOG COMPUTER, ELECTRONIC ASSOCIATES, INC., LONG BRANCH, NEW JERSEY

The EAI HYDAC Series 2000 Hybrid Digital/Analog Computer introduces a new concept to engineering and scientific computation by providing the engineer with a single computer that he can easily operate alone and apply either analog or digital techniques as desired to the solution of the problem. The costly process previously practiced in attempts at hybrid computation – that of combining a complete digital data processing computer with an analog computer – has been refined considerably and made economically practical. Analog and digital operations are now combined in one centralized system to achieve a computational efficiency that is well beyond the limits of either analog or digital computers used alone. The traditional advantages of both analog and digital computers – the analog computer's speed, lower cost, and ease of programming and the digital computer's unique capacity for data storage and time sharing of components – have been combined to expand problem solving capabilities at lower cost.

Since many of the digital operations required for hybrid computation schemes involve mainly those of timing, selection, sequencing, memory look-up, and calculation of simple functions, such schemes can be accomplished without the expense of large data processing digital machines. Digital operations can become an integral part of the expanded general purpose analog computer making them available to computer laboratories that have no digital computers, or during those periods when time is not available on the latter. With HYDAC Series 2000, analog and digital computation can be centralized in a single laboratory thereby eliminating scheduling and training difficulties.

Programming of the entire system parallels closely the relatively simple operation of the analog computer. The transition from the use of relays and switches in the general purpose analog computer to logic devices is made very easy. Extensive retraining of analog programmers is unnecessary.

Analog operations of summation, inversion, continuous integration, multiplication, division, and function generation are performed by a proven computing system. All electronic, wide bandwidth computing components insure high dynamic accuracy for real-time or repetitive mode of operation. Multiplication and other nonlinear operations are performed with signal frequencies in the kilocycle range, so as to realize full advantage of the high-speed digital circuits.

Digital Computing Components

Digital computing components are general purpose in concept and design. Five major groups of components are available to provide programmed digital logic, digital memory, analog memory, analog digital conversion, and advanced digital arithmetic. Each of these groups of components could be the complete justification for HYDAC Series 2000, however, a more powerful and useful system is one that combines several of the major classes of digital components.

Modular designed digital building blocks permit fullest advantage of the economy and flexibility of the pre-patch panel concept to be realized. Digital switching circuits employing one basic type of universal gating circuit for maximum flexibility and added economy are

used to perform basic digital operations. Completely solid state with 20-megacycle switching capabilities these basic modules are combined on printed circuit cards to form more complex operations.

The 2000 is the result of a comprehensive design study by experienced computer users, programmers, and designers who are concerned with the basic requirements of hybrid computation.

Major components of the 2000 are a general purpose analog computer and a digital console. This console is designed to take fullest advantage of the economy and flexibility of the pre-patch panel concept; modularized digital building blocks capable of performing basic digital operations plug into standard connectors behind the patch panel, and each is terminated in a four-by-ten hole area of the patch panel. The digital building blocks are interchangeable. HYDAC Series 2000 may be made to have many different capabilities by employing different combinations of building blocks. This flexibility is obtainable without prejudice to design or wiring of the digital console. Reliability, economy, and ease of maintenance result from all solid-state design.

Digital operations in the 2000 are assembled from the following console units and groups of digital computing components.

Digital Console

With provisions for mounting the digital computing components, the basic console unit provides power supplies with necessary wiring, facilities for control and slaving of the unit to the analog computer, selector switches, flip-flop indicator lights, and control buttons, etc., and the 3450-hole pre-patch panel system. A clock unit with timing signals terminated on the patch panel provides control timing and synchronization for the entire system. Console expansion units available include a punched-paper-tape input-output system, a decimal-binary conversion system and special control units.

Logic Building Blocks

Logic components are very high speed (50 nanoseconds switching time), solid-state switching circuits, each designed to provide specific logic functions. A wide choice of functions is available, as well as a choice of the level of logical organization, such as: logic gates, RST flip-flops, 4-bit shift registers, monostable multivibrators, up-down counters, preset counters, ring counters, BCD counters, differentiators, buffer registers, adders, multipliers, special control units, and timing units.

Digital Memory Building Blocks

High-speed digital memory units, known as serial memory units, are available in four different sizes with circuits to make it possible to provide control directly from the patch panel and to connect the units together for special functions.

Analog/Digital Converters

These building blocks convert control signals and analog voltage signals from analog to digital, and back to analog. High-speed electronic switches and incremental converters, as well as conventional whole number converters, are also available to satisfy additional conversion requirements.

Analog Switching and Memory

These building blocks consist of MICRO-STORE memory and switching modules which are operated in combination with analog operational amplifiers to provide high-speed point storage of analog voltages plus electronic switching capabilities.

Advanced Digital Arithmetic Units

These digital building blocks consist of accumulators, adders, summers, input units, constant storage units, and comparators. These units provide the analog computer with expansion units capable of high precision computations.

Applications

The combination of analog and digital operations not only allows more economic analysis of certain classes of engineering and scientific problems, but in some instances is a far superior method of analysis. Although the range of applications of the analog computer is indeed wide, the additional ability to store, to process data, and to use the results of this processing as input data for further calculations extends the scope of application of the analog machine. HYDAC Series 2000 provides these capabilities and thus increases the range of problems that the analog computer can

solve economically. It gives new meaning to high-speed computation.

Among the more important applications of this new computer are:

Iteration and Optimization Studies

Problems of this nature arising in model building, process simulation, parameter studies, and end-point boundary value systems can be optimized by trial and error methods. Computation time is significantly reduced by the incorporation of suitable logic and switching functions to allow the analog computer to pro ceed automatically through a complete iteration procedure until an optimum is found. The same logic functions facilitate the automatic programming of parameter searches, performance curve fitting, and matching of boundary values.

Partial Differential Equations

The solution of many scientific problems is represented by the solution of linear or non-linear partial differential equations. Solutions based on difference techniques utilizing function storage and playback permit equipment savings through the time sharing of analog circuits. Such techniques allow the time-domain simulation of field problems where space variables are replaced by high-speed time sweeping, while the physical analogy of time is preserved. Hybrid operations also facilitate the solution of boundary value partial differential equation problems by the method of characteristics or by integral equation methods through the use of serial solution techniques and time multiplexing.

Simulation of Logic Functions

Often a problem being studied is partially represented in its physical description by decision functions. Such problems occur with increasing frequency in the study of space vehicle characteristics and the control of complex processing. A prime example is the simulation of an adaptive control system. Here the dynamic behavior of the system being controlled is represented by normal analog elements while the logic of the control system is represented by the available digital logic elements.

Integral Equations

This important class of equations, whether arising directly or indirectly as in the solution of partial differential equations, can be solved efficiently by a combination of analog and digital elements. Simpler investigations, such as those involving the solution of the Volterra and Fredholm integral equations, can be programmed easily using general purpose elements. More complex solutions now become economically attractive.

Auxiliary Mathematical Functions

Special operations such as multiplications, transport delay simulation, function generation, slow integration, etc., may be custom designed, with suitable programming, for combined operations with analog elements.

Problems which have been programmed for solution with the 2000 at EAI's Princeton Computation Center include:

1. A generalized optimization control program to optimize any non-linear function of n variables that is programmed for an analog computer.

2. An eigenvalue problem for determining the normal modes of a vibrating beam.

3. A reaction-jet space capsule control problem.

4. Iteration solution of tubular reactor and control system design problem.

5. Solution of partial differential equations by the method of characteristics.

6. Integral equation solution of a boundary value problem.

IBM 7094—INTERNATIONAL BUSINESS MACHINES CORPORATION, WHITE PLAINS, NEW YORK

The IBM 7094 data processing system is the most powerful in the company's line of intermediate- and large-scale solid-state scientific computers. This line also includes

the 7040, 7044, and 7090. Increased speed and processing power of the 7094 are provided by faster adding circuitry, additional index registers and instructions, and the facility for performing double-precision floating-point arithmetic.

The new system is offered in a wide variety of input-output configurations and has storage capacity of 32,768 words. It can be linked to various IBM Tele-processing devices for full data transmission ability. A library of 7094 programs covering a wide range of computer functions is provided at no cost by IBM. System compatibility enables a customer with a 7090 to use his new 7094 with virtually no reprogramming.

The memory reference cycle is 2.00 microseconds for the 7094, compared to 2.18 microseconds for the 7090. When processing is performed in the floating-point mode (generally used when the numbers involved vary greatly in magnitude), the 7094 can perform mathematical computations 1.4 to 2.4 times faster than the 7090, depending upon the technique used to solve problems. Memory reference speeds for IBM's intermediate- and large-scale scientific systems are as follows:

System	Memory Reference Speed (μsec)
7094	2
7090	2.18
7044	2.5
7040	8
709 and 704	12

Modular design provides upward compatibility of these systems. A user can enlarge his system or advance to a more powerful computer with a minimum of reprogramming.

A team of IBM customer engineers can expand a 7090 which is already on rental to a 7094 in the user's office within 72 working hours, including installation and system testing. The changeover involves installation of a higher-speed processing unit containing faster solid-state adding circuitry, additional instruction circuitry to accommodate new commands, and four additional index registers. Faster circuitry is installed in other elements of the system and a display panel for the additional index registers is mounted on the operator's console.

Input-Output

IBM 1301 disk storage units and Hypertape magnetic tape drives can be linked to the system for high-speed input and output of data. Up to five 1301's with a combined capacity of 279 million characters can provide additional storage on magnetic disk files.

Up to 20 Hypertape units, capable of reading data from and writing data on tape at the rate of 170,000 characters a second, or up to 80 IBM 729 tape units, ranging in read-write speed from 41,700 to 90,000 characters a second, can be linked to the system. Various combinations of Hypertape and 729 tape units can be used with a single 7094.

An IBM 1011 paper-tape reader, capable of reading data into the computer at the rate of 500 paper-tape characters a second, enables the system to accept data transmitted directly by teletype. Common carrier telegraph equipment can also serve as remote input-output devices for the system.

Ability to transmit and receive data over long distances in computer language is provided by the IBM 1009 data transmission unit. This IBM Tele-processing device enables the 7094 to communicate over leased telephone or telegraph lines with another computer (7094, 7090, 7040, 7044, 1401, 1410), a magnetic tape transmission unit or a card transmission unit at speeds up to 300 characters per second.

The 1014 remote inquiry unit, another IBM Tele-processing device, is equipped with and input-output typewriter and can be used for direct interrogation of the computer from a point up to 8 miles away.

Programming Support

A number of 7090/94 programming systems and languages will be provided by IBM to 7094 users without charge. The 7094 is so designed that programs written for the 704, 709, 7040, 7044, and 7090 can be run with a minimum of modification and at higher speed. 7090/94 programs provided by IBM are:

FORTRAN

The widely accepted IBM FORmula TRANslation system enables the user to write his programs in a language closely resembling that of mathematics. Thus scientists and mathematicians can code problems with a

minimum of computer knowledge. The FORTRAN Assembly Program converts these coded instructions into machine language.

COBOL

This COmmon Business Oriented Language permits the user to write programs using familiar business terms. COBOL is the result of work by the Conference on Data Systems Languages (CODASYL), a voluntary effort of various computer manufacturers and users under sponsorship of the Department of Defense. The COBOL processor converts English-like instructions in COBOL language into a machine-language program.

Input-Output Control System

IOCS relieves the user of having to write repetitive input-output instructions for every program. It provides a complete set of instructions for effective use of all input-output devices, including the 1301 and Hypertape.

Sort

This program facilitates automatic reorganization of data stored on magnetic tape.

9PAC

Designed for business applications, this programming system provides for the establishment and maintenance of data files and the production of reports with a minimum of programming effort.

Basic Monitor (IBSYS)

This system permits uninterrupted processing of any of the above programs written for either the 7090 or the 7094. It calls programs into use from a tape library and enables them to take full advantage of whichever input-output devices are linked to the system.

Commercial Translator

Designed for commercial data processing applications, it enables the user to write his programs in a language based on English.

A typical IBM 7094 sells for $3,134,500 and rents for $70,000 a month. Installation of the 7094 will begin in the fourth quarter of 1962. The new system is manufactured at the company's Poughkeepsie, New York, plant.

900 SERIES COMPUTERS—
SCIENTIFIC DATA SYSTEMS,
SANTA MONICA, CALIFORNIA

The Scientific Data Systems 900 Series of computers consists of three general-purpose digital computers – the 910, 920, and 930. This article primarily describes the first two, the 930 is only briefly treated. All the computers in the series are intended both for special-purpose system integration and for general-purpose scientific use. All sell for under $100,000.

The computers operate with a 24-bit binary word; a twenty-fifth bit provides a parity check on all memory operations. Fourteen bits of the instruction serve to address up to 16,384 words of random access core storage; 6 bits are used for the operation code. One bit is used to signify that the address is indirect; that is, that the effective address is to be found in the location specified by the address portion of the given instruction. The location thus specified may, in turn, contain an indirect address bit. The number of iterations of this process is not limited. Another bit adds the contents of an index register to the address prior to execution of the instruction. If an indirect address bit is present, the effective address is found in the location that results after indexing. A relative address bit is also provided in order to simplify the loading of sub-routines, etc. The final bit in the instruction is used to signify that the operation code is to be interpreted as a Programmed Operator. This requires some explanation.

There are many practical advantages to be gained from designing a series of computers such that programs for any given computer, within the limitation of memory size, can be run by any other computer in the series. For example, within a given facility a number of different computers can be employed, each of an appropriate size. If any one of these is unavailable, another can be directly employed without extensive reprogramming. This program compatibility is relatively simple to mechanize if the programs from a smaller computer are run on a computer with an

instruction repertoire that, loosely speaking, contains the smaller computer's instructions as a subset. It is the inverse problem that the programmed operator is intended to solve. The presence of the programmed operator bit causes the operation code to be interpreted as a sub-routine entry address. Thus larger computer instructions that do not exist in the smaller computers are interpreted directly by sub-routines in the smaller computers. As a result, all programs for the 900 Series are interchangeable, that is, the computers are "symbolically homogeneous." An example will clarify this term. All three 900 Series computers use different multiply commands. The 910 has only MULTIPLY STEP, the 920 has MULTIPLY, while the 930 has FLOATING POINT MULTIPLY as well as MULTIPLY. In running a 930 program on the 910, for example, the FLOATING POINT MULTIPLY command is identified by the loader as a programmed operator and, upon execution of this command, the operation code is interpreted as the address to which the program transfers in order to pick up the appropriate floating-point multiply sub-routine.

In addition to providing symbolic homogeneity, the programmed operator serves to extend the command list of any of the 900 Series computers for a given application. For example, in some classes of programs, complex arithmetic instructions are useful. The symbol, ADJ (Add Complex), can be assigned an instruction code and the address portion used to specify the location of the real part of the operand. The imaginary part is stored in the adjacent memory cell. This instruction code will cause a program transfer to the sub-routine while storing the return address.

Although all programs are interchangeable, the time and memory requirements for a given problem vary among the three computers. The basic execution time for addition is 16 microseconds for all computers, including indexing and all memory accesses. The 920 requires 128 microseconds to produce a 47-bit product from two 24-bit factors including memory accessing and indexing; the 910 requires 248 microseconds. The floating-point (39-bit mantissa, 9-bit exponent) sub-routine set requires 90 words and approximately 800 microseconds per floating-point operation in the 920, while the 910 requires 180 words and approximately 3000 microseconds per instruction.

Input-output is probably one of the most critical design problems in low-cost computers that are to be used for both systems and general scientific computing. All 900 Series computers have identical input-output logic which incorporates five separate methods of operation:

Single Bit Control

Up to 16,000 different control signals can be generated or tested by the 900 Series computers. For example, a single instruction starts a specific magnetic tape unit, indicates the number of characters per word, and the buffer that is involved. A single instruction can also test the state of the breakpoint switches, the parity error detector, or any other signal, and skip as a function of the result.

Input-Output Buffer

A full word plus one character buffer is provided which accepts and transmits words between the memory and external devices. The extra character minimizes timing problems and so increases programming efficiency. The buffer operates upon characters of up to seven bits, generates and checks parity, and operates simultaneously with computation. A program interrupt is provided to facilitate this simultaneity. The program control automatically transfers to an input-output processing routine when the buffer either is empty during output or contains a word during input. Using this scheme, 15 kc character rate magnetic tape information can be processed while permitting the computer to operate 64 percent of the time on other programs. The maximum transfer rate is 41.6 kc. Because the buffering hardware is integral to the computers, the cost of magnetic tape units is minimal. The 15 kc tape units for the 900 Series are under $20,000.

As an optional feature, a second and identical buffer is available for applications that require simultaneous input and output. Using this buffer, for example, a gapless magnetic tape can be read and an IBM-format tape written, simultaneously, at a rate of up to 5 kc.

Parallel Input-Output

In operating with certain devices such as printers, analog-to-digital converters, and display systems, it is more convenient to process words than characters. For these cases, the computer can transmit or accept 24 bits in parallel along with an interlock signal to synchronize the transfer. A 25th bit is provided for parity information. Using this

parallel transfer method, several 900 Series computers can be interconnected to perform complex tasks that are beyond the capabilities of any single computer. The maximum transfer rate is 62,500 words per second.

External Memory Interlace

The memories of the 900 Series computers can be time-shared between the computer proper and external devices. Prior to accessing memory for each instruction, the computer automatically tests to see if an external device, such as a magnetic tape unit, requires access to the memory for either input or output. If access is required, the computer is halted for the 8 microseconds necessary to transfer a word and computation is then resumed. Character transfer rates of up to 124 kc are possible with the computer operating and 500 kc with the computer in HALT. An unlimited number of buffered input-output devices may be connected to a 900 Series computer using this technique. A 30 kc magnetic tape unit with automatic search is one such device that is available.

Priority Interrupt

An optional feature of the 900 Series is a priority interrupt system with up to 1024 channels in blocks of 16. Each channel causes the computer to interrupt to a unique memory location. Each channel has an assigned priority status such that, when it is activated, it causes the interruption of previous interrupts of a lower status and, in turn, it is interrupted by channels of higher status.

The number of input-output devices that can operate with any of the 900 Series computers is essentially unlimited. Any number and combination can be employed. In addition to the magnetic tape units already discussed and the high-speed, paper-tape punch and reader and typewriter provided as standard equipment, card readers, printers, disc files, analog-to-digital converters, and digital-to-analog converters are available.

Special power failure protection is provided on all computers. Special sensing devices sense the status of the ac-input line before each memory operation and halt the computer if the line is low or if power has failed. With priority interrupt, this sensing system can be used to store all registers before the dc-power fails. The computer can then simply be restarted when power is again available.

A typical system that illustrates the speed, memory efficiency, and input-output flexibility of the 900 Series is the general data acquisition and evaluation problem. Analog data is multiplexed and converted to digital form under the control of the computer. The resultant data is entered into the computer and compared with high and low limits. A linear transformation is then performed in order to eliminate zero and full-scale errors and, at the same time, to translate the raw data into engineering units. The program to perform these operations requires 29 instructions in the 910 and approximately 600 microseconds per point. In the 920, 17 words and 300 microseconds per point are required.

In construction, the 900 Series is unique for nonmilitary computers in that only silicon semiconductors are employed. The 910 uses approximately 900 transistors and 800 watts of power, while the 920 has 1100 transistors and requires 1000 watts. No air conditioning is needed in either case since the computers will operate in ambients of from 0° to 55°C.

A complete software system for the 900 Series includes a utility package, a symbolic assembler, and a FORTRAN-compatible compiler. The latter is similar to the IBM 1620 FORTRAN II compiler with the addition of magnetic tape statements. Again, because of the symbolic homogeneity of the 900 Series computers, any of the computers can be employed for compiling and the resultant object program run on any other of the computers.

SDS 900 SERIES CHARACTERISTICS

SDS 910 Computer

24-bit word plus parity bit
Binary arithmetic
Single address instructions with:
- Index register
- Indirect addressing
- Programmed operators

Basic core memory 2048 words expandable to 16,384 words

Typical execution times (including memory access and indexing):
- Add ---------- 16 μsec
- Multiply ---------- 248 μsec
- Floating-Point Operations:
  - (39-bit Mantissa + 9-bit Exponent)
    - Add ---------- 1984 μsec
    - Multiply ---------- 2600 μsec

Program interchangeability with other SDS 900 Series computers

Parity checking of all memory and input-output operations

1024 channels of priority interrupt (opt'l)

Memory nonvolatile with power failure

Input-Output:
- Standard:
  - 300 character/second paper tape reader
  - Program interrupt
  - Display and manual control of internal registers
- Optional:
  - 60 character/second paper tape punch
  - Automatic typewriter
  - Magnetic tape units (IBM compatible)
  - Line printer
  - Punched card equipment
  - Direct communication with IBM 7090
  - A/D converters, etc.

Buffered input-output at rates in excess of 80,000 characters/second

FORTRAN II and Symbolic Assembler as part of complete software package

All silicon semiconductors
0° to 55°C operating temperature range
Dimensions: 75 × 24 × 27 in.
Power: 110v, 60 cps, 8 amps

PRICE: $41,000

SDS 920 Computer

24-bit word plus parity bit
Binary arithmetic
Single address instructions with:
- Index register
- Indirect addressing
- Programmed operators

Basic core memory 4096 words expandable to 16,384 words

Built-in Floating-Point Instructions

Multi-precision Instructions

Typical execution times (including memory access and indexing):
- Add ---------- 16 μsec
- Multiply ---------- 128 μsec
- Floating-Point Operations:
  - (39-bit Mantissa + 9-bit Exponent)
    - Add ---------- 368 μsec
    - Multiply ---------- 560 μsec

Program interchangeability with other SDS 900 Series computers

Parity checking of all memory and input-output operations

1024 channels of priority interrupt (opt'l)

Memory nonvolatile with power failure

Input-Output:
- Standard:
  - 300 character/second paper tape reader
  - 60 character/second paper tape punch
  - Automatic typewriter
  - Program interrupt
  - Display and manual control of internal registers
- Optional:
  - Magnetic tape units (IBM compatible)
  - Line printer
  - Punched card equipment
  - Direct communication with IBM 7090
  - A/D converters, etc.

Buffered input-output at rates in excess of 80,000 characters/second

FORTRAN II and Symbolic Assembler as part of complete software package

All silicon semiconductors
0° to 55°C operating temperature range
Dimensions: 66 × 48 × 27 in.
Power: 110v, 60 cps, 10 amps

PRICE: $89,000

BRLESC—U.S. ARMY BALLISTIC RESEARCH LABORATORIES, COMPUTING LABORATORY, ABERDEEN PROVING GROUND, MARYLAND

Introduction

The complement of large-scale, digital, electronic, general-purpose computers now consists of the EDVAC, ORDVAC, and the new Ballistic Research Laboratories' Electronic Scientific Computer (BRLESC), which just recently has been placed in full service. BRLESC was designed, developed, and assembled by BRL's Computing Laboratory Engineers, Mathematicians, and Technicians, from contractor-provided components. The scientific computational workload of BRL is gradually being shifted to the BRLESC. Many important old problems can now be solved in a small fraction of the time formerly required. Some problems which were previously unsolvable on EDVAC and ORDVAC because of limited speed and storage capacities, are being readily solved by the BRLESC. The BRLESC has 4096 words of magnetic core storage with a 0.6 microsecond access and 1.2 microsecond cycle-time, 63 index registers, a 68-bit word length, fixed- and floating-point logical and arithmetic operations, and an extremely rapid compiler. A three-address instruction requires about 5 microseconds. A fast-carry logic 1-microsecond parallel digital adder is used. A selection of off-line conversion from and to various media including cards, tapes, and printer is available.

A BRLESC high-speed digital computer compiler (FORAST) has been coded and checked. This compiler is a machine-language set of instructions that accepts programs which are written in any of three languages or any combination of the three. The languages are:

1. Mathematical formula and English statement language,

2. BRLESC symbolic language, and

3. BRLESC absolute language.

This BRLESC compiler language is compatible with the ORDVAC.

The preparation of aiming data for free rockets, one of the missions of the Computing Laboratory of the Ballistic Research Laboratories, is based on the reduction of data from flight tests; that is, the mathematical simulation of each such test. The advent of BRLESC with its great computational speed has permitted the introduction of vastly more precise and sophisticated techniques in these reductions, resulting in a more complete mathematical model of the rocket being considered with consequent increase in accuracy of the aiming data provided for it in the form of a firing table.

Origin of BRLESC

In 1956, BRL transferred $100,000 to the National Bureau of Standards (NBS) to assist in the development of universal logical packages which could be used in the construction of a new, fast, reliable, scientific computing machine. A logical package is a group of decision making circuits which are capable of developing a certain result in accordance with conditional input statements. For example, one type of element "agrees" that an entire statement is true if all of a group of conditions are fulfilled; another type yields a "true" signal if only one or more of the conditions are met. With these, coupled with the ability to reverse a decision, all the arithmetic, logical operation, and number manipulations may be performed with reasonable economy of electronic parts.

At the time the funds were transferred, NBS was committed to the design of their new PILOT Multi-Computer System. The funds assisted the Bureau in arriving at a tentative design of arithmetic, logical, and control units. After tests by BRL, certain changes in the design of the logical package were requested.

Modifications of the logical packages were approved by NBS. In February 1958, the sum of $175,000 was transferred to the Bureau to cover the cost of 6000 packages for BRL, to be procured along with the NBS's own requirement for PILOT. At this time BRL's programming staff prepared a description of the instructions to be automatically executed by BRLESC. Due to various considerations – the different types of application, desire for easy programming, and overall economy – BRL and NBS parted ways in development. All that there is in common today between BRLESC and the NBS computer is the logical package and aspects of the high-speed arithmetic unit. BRLESC is using high NBS-proposed high-speed carry logic. BRLESC's instruction code, physical construction, internal arrangement, control logic, peripheral equipment, and many other aspects are different.

High-speed carry logic is an improved method of licking a problem that confronts

anyone who adds a column of figures. Whether it is a third-grader or BRLESC, the matter of "one to carry" can be a poser, both from the standpoint of getting the right result, and of the time required to get it. In the human case, a person doing the sum 9999 plus 1 recognizes the "one to carry" aspect as universal, and jumps forward to the answer 10,000 instantly. In a rough way this type of thing is also involved in the BRLESC high-speed carry logic design. Thus, the computer recognizes whether there will be a carry or not in all columns at once, for after all, either there is a carry or there is not. If there is, it can only be a one. A carry cannot propagate past a sum digit which is ZERO; therefore, signals can be generated to indicate at which digit positions a carry should be generated, in far less time than it would take to wait and see if there is a carry propagated from all previous digit positions during a summation.

BRLESC's High-Speed Storage Unit

The high-speed storage unit developed for use in BRLESC represents a new step forward in the development of computer components. The development contractor – Ampex Computer Products Co – has delivered this unit, not only to BRL for use in BRLESC, but has furnished similar units to a number of computer manufacturers for integration into their own systems to meet other defense requirements. It furnishes a current example of how Ordnance requirements have been met, with corresponding benefits to other defense activities.

Construction cost accounts of most large-scale, electronic, digital computing systems reveal that the high-speed storage element is the most expensive single item. This is the section of the computer which "receives, stores, and issues" information and instructions in the form of computer numbers or "words." BRLESC uses a high-speed magnetic core storage unit having a capacity of 4096 words, of up to 72 "bits" each (64-bit numbers are used). The translation of these bits into decimal terms is equivalent to approximately 19 decimal digits. Such long word length is necessary to provide the extreme precision required of calculations made in connection with scientific research. For many other types of application, such as ordinary commercial calculations, such a high degree of precision is not required and is not incorporated in many of today's computers.

The capability to handle long words carries with it a requirement that the computer be able to make use of them very rapidly. The complete read-write cycle time of the BRLESC memory is 1.5 microseconds, which is the fastest large-scale memory in operation today. BRLESC is approximately one-half as fast as the two fastest high performance computers yet constructed[1] anywhere, and twice as fast as the most rapid computer currently available commercially.[2] The faster machines use overlapping memory cycles from separate banks of memory to achieve high effective memory speed. This cycle time is important, since three to four cycles may be required when the computer adds two numbers. Even though the elapsed time for one cycle is only 1.5 millionths of a second, this value becomes critical when a long series of computations are undertaken. The computer executes instructions in the form of a huge number of small steps, each requiring a specific time interval to perform. These many small steps run into the billions for typical problems.

In view of the time required for delivery of the proposed high-speed storage element, the Chief of Ordnance gave early approval to the contract with Ampex Computer Products Company. After certain delays due to technical difficulties, the operational unit was delivered to BRL on May 15, 1961, at a total cost of $680,000, including supplements, under Ordnance Contract No. DA-04-495-ORD 1500. The resulting storage element represented a major step forward in computer components. As stated above, the advance was immediately incorporated into other computer designs. Approval has been obtained to increase the storage capacity to 12,288 words.

Other BRLESC Features

BRLESC was designed primarily for the solution of scientific problems in which high computational speed and high precision are required. It may be programmed to perform any task amenable to numerical methods of solution. The binary system is used exclusively in the arithmetic unit of the machine. This is the system mentioned previously, in which decimal numbers (to the base 10) are converted into binary numbers (to the base 2) which yields a long string of ONES and ZEROS. A BRLESC program will convert decimal input information

[1] BRLESC is roughly 1/2 the speed of LARC and roughly 1/3 the speed of STRETCH

[2] IBM 7090, which is 1/4 the speed of LARC and 1/6 the speed of STRETCH

into binary form for computational purposes and then convert the results to decimal form for output, for the convenience of the user.

To supplement the high-speed storage element, magnetic drum storage units will be installed as back-up memory. It is expected that the capacity of the drums will be about 35,000 words.

BRLESC has facilities for reading cards, punching cards, reading magnetic tape, and recording on magnetic tape. A maximum of 16 magnetic tape handlers are directly accessible to the programmer. Any two magnetic tape handlers, one drum, the cardreader, and the cardpunch may be operated concurrently under separate automatic controls.

Access to information by the computer is an important aspect of its value. Time is required to put information into the computer, and to print or otherwise record the results of its calculations. In fact, computers make the actual calculations so rapidly that the input and output aspects can be troublesome, that is, slow, tedious, mechanical motions of masses of stored data and instructions. In the case of BRLESC, information may be transferred to the machine via punched cards or magnetic tape. The actual information read into BRLESC may be a straight binary number, a binary coded decimal number, a binary coded group of alphabetic characters, or, broadly speaking, any type of binary coded information that the programmer desires.

Another valuable feature of BRLESC is its ability to change addresses in instructions by fixed amounts, automatically. A simple analogy is the case of the village postmaster who asks his assistant to put a certain circular in every pigeonhole postbox in the office. The assistant will not need to be told specifically to first fill box one, then box two, then three, and so on. One direction will be sufficient. A more complicated analogy is the bank clerk making up a table of monthly payments on loans of various sizes, interest rates, and repayment periods. If he is capable, he will progress from one to another without requiring new instructions. After computing the payments for a 5% loan of $10,000 payable in 10 years, he will repeat the calculations for 5-1/2%, then 6% and for terms of 15, 20 and 25 years and so on.

This feature of BRLESC, which is called indexing, permits the programmer to use the same set of instructions to process as many sets of data as he desires, simply by changing the index value, instead of modifying the basic overall instructions. The details of modifying index registers, counting, or jumping to a different set of instructions, to cite a few examples, are sometimes referred to as "housekeeping." BRLESC has been designed so that most of this housekeeping work can be done concurrently with arithmetic operations. For example, while BRLESC is performing a single multiplication operation, as many as four "housekeeping" instructions may be processed independently of the arithmetic unit, at a great saving of time in the overall computations.

As indicated, BRLESC operates in response to an internally-stored program of detailed instructions. Arithmetic and logical operations can be performed on these instructions, permitting instructions to be altered in accordance with the results thus far obtained during the course of the program. For example, the computer might work on evaluating a complex electrical circuit, expressed in mathematical terms, to determine what the value of current would be at a certain point X in the circuit. Let us assume that 5 amperes is the maximum current value tolerable, in the actual physical case. The computer can be relied upon to examine the current value it computes, and do one thing if this value is less than 5 amperes, or another thing if the value is greater than 5 amperes. In one actual case it was desired to determine whether a certain machine gun previously used on a tank could be adapted to mounting on a helicopter. A machine gun must have a sufficient recoil velocity so that between shots there is enough time for the firing mechanism to be cocked and a new cartridge properly chambered. Recoil involves action and reaction between gun and its mount. Thus a gun mounted on a tank, on a heavy mass, will have a faster recoil than when mounted airborne fashion on a relatively light helicopter. The computer doing calculations of recoil velocity was able to appraise the various results obtained, and then make new calculations with new or modified instructions, automatically, based upon these initial results. The ability of the computer to modify its own instructions, along with the indexing feature, saves writing countless thousands of additional instructions in complicated problems.

BRLESC Potential

What actually will BRLESC do for the Ordnance Corps and the scientific community? It will permit the solution of problems which could never be solved before, due to the excessive amount of time or space required; and it

will provide a precision not usually possible without the great pain of multi-precision arithmetic. BRLESC will be used in the computation of firing tables and guidance control data for Ordnance weapons, including missiles. It will handle interior ballistics problems, for example, the behavior of projectile, propellant, and launcher; stability and thermodynamic properties of rocket propellants; reflected shock waves; vibration of gun barrels; and flow of fluids through porous media.

Terminal ballistics studies to be performed include nuclear, fragmentation, and penetration effects, in such areas as explosion kinetics, shaped charge, ignition, and heat transfer.

Ballistic measurement studies to be performed will include photogrammetry, ionospheric measurements, damping of satellite spin calculations, reduction of satellite doppler tracking data, and computation of satellite orbital elements. Other studies will comprise anti-aircraft and anti-missile evaluation, war-gaming problems, linear programming for solution of Army logistical problems, probabilities of mine detonations, lethal and kill probabilities of mine detonations, and lethal area and kill probability studies of rockets and guided missiles.

History of BRL Computers

At the beginning World War II, the Ordnance Department had the sole responsibility for providing the principal scientific and logistic support for the Army.

The only scientific facility available to them for carrying out these experiments with weapons was the Ballistic Research Laboratory at Aberdeen Proving Ground, Md. Its computing group was staffed by a handful of well trained and highly skilled civilian employees of the Ordnance Department. The laboratory was responsible for the preparation of artillery firing and aircraft bombing tables for the Army and the Army Air Corps. They also obtained experimental data of high accuracy and precision, necessary to the computation of the firing and bombing tables.

This group of scientists at the Proving Ground had available to them at the time an important calculating device, the Bush differential analyzer. This continuous variable calculator had been installed at the Proving Ground about 5 years earlier.

This analyzer, consisting of ten integrating units and two output tables, was an important mechanical aid to computation. Despite its capability and value, the analyzer had several severe limitations. Probably the most severe of these was the mechanical torque amplifier, which frequently failed toward the end of a long trajectory run with the loss of the preceding computations.

ENIAC (Electronic Numerical Integrator and Computer)

In 1942 the United States was locked in bitter combat with the Axis Powers. It was imperative that a faster calculation method be devised to provide the troops with firing tables for the many new weapons being developed.

The Moore School of Electrical Engineering believed that they could utilize electronics and develop a computing machine. The Ordnance Corps awarded them a contract for the design and construction of an electronic computer.

In 1947 the completed computed was installed at BRL. The latest thing in computers at that time, the ENIAC, was a decimal machine utilizing 19,000 vacuum tubes, 1500 relays and hundreds of thousands of resistors, capacitors, and inductors. It had 30 separate units weighing more than 30 tons. In calculating a 60-second trajectory, ENIAC completed the job in 30 seconds, half the time of the actual flight of the projectile from the gun to the target.

EDVAC (Electronic Discrete Variable Automatic Calculator)

The urgent need for an operational computer had made it necessary to freeze the engineering design of the ENIAC early in the game. It was agreed upon between BRL and the Moore School of Electrical Engineering at the University of Pennsylvania that, as work on ENIAC permitted, the design and construction of an improved computer should be pushed forward. The EDVAC, with greater flexibility and better mathematical performance, was installed at BRL in 1949 and placed in operation in 1950.

The major features of this computer were: use of the binary system (rather than the

decimal system of numeration that had been used in ENIAC), serial arithmetic mode (improved means of transferring numbers from one part of the computer to another), a four-address instruction (permitting a total of 16 different commands to the computer), and duplicate circuitry for check purposes. EDVAC was the first internally-stored program computer to be built. With an internally-stored program device, the "pattern of interconnections" is set up by the computer itself, on command. The program at any given time can be recorded on magnetic tape, a form of "memory" for the computer. Reversing the process, the tape can be fed back into the computer at any time and all of the previous programs or "interconnections" will be reestablished. This is of obvious advantage when work on one problem must be momentarily suspended in favor of another, not to mention the simplicity with which programs may be modified during the course of a computation, based on results obtained thus far. Thus the computer makes its own decisions, according to what it has discovered. This represents a great breakthrough in computer design concept.

Work on the EDVAC stimulated design and construction, by other groups of a large family of similar computers, including SEAC, DYSAC, MIDAC, FLAC, and the later UNIVAC's.

Next in line of development was the ORDVAC, a parallel binary computer which in turn spawned a new group of computers - ORAC, ORACLE, JOHNNIAC, ILLIAC, SILLIAC, MANIAC, CYCLONE, ERA 1103 (UNIVAC Scientific), and IBM 701, that were constructed by many organizations in government, industry, and education.

These designs constituted little, if anything, new in computation design, but carried out existing design principles using the ever advancing technology of electronics. During the early 1950's a major part of the scientific computational workload of the Western world was accomplished on these machines.

ORDVAC (Ordnance Variable Automatic Computer)

ORDVAC was constructed by the University of Illinois for the Ballistic Research Laboratories at the Proving Ground, under a contract from the Ordnance Department.

The machine was originally designed to solve the following types of problems:

1. Exterior ballistics problems such as high altitudes, solar and lunar trajectories, computation for the preparation of firing tables, and guidance control data for Ordnance weapons, including free flight and guided missiles.

2. Interior ballistics problems, including projectile, propellant, and launcher behavior.

3. Terminal ballistics problems, including nuclear, fragmentation, and penetration effects in such areas as explosion kinetics, shaped charge behavior, ignition, and heat transfer.

4. Ballistic measurement problems such as photogrammetric, ionospheric, and damping of satellite spin calculations, reduction of satellite doppler tracking data, and computation of satellite orbital elements.

5. Weapon systems evaluation problems, such as antiaircraft and antimissile evaluation, war game problems, linear programming for solution of army logistical problems, probabilities of mine detonations, lethal area and kill probabilities of mine detonations, and lethal area and kill probability studies of missiles.

ORDVAC is a general purpose computer capable of carrying out individual arithmetic operations at high speed using a parallel binary number system, in an asynchronous manner. Originally, the ORDVAC operated with an electrostatic storage unit. This has since been converted to a magnetic core storage unit, with increased speed and capacity.

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COMPUTING CENTERS

RECORDING PHYSIOLOGICAL MEASUREMENTS FOR DATA PROCESSING—NATIONAL BUREAU OF STANDARDS, WASHINGTON 25, D. C.

A method for using computers to study the reactions of the human body to psychological stimuli has been developed at the National Bureau of Standards. The method employs equipment that accepts simultaneous, rapidly occurring psychophysiological measurements in analog form, converts them to digital form, and records them on magnetic tape for later computer processing. The electronic circuits to drive and interconnect a standard analog-to-digital converter and recorder were designed for the Air Force Office of Scientific Research by a team which included E. S. Sherrard, of the NBS data processing systems division and Herbert Zimmer, psychologist at the University of Georgia. Although intended to record the responses of subjects in a continuing psychological investigation, this equipment can be useful for multichannel recording in many biological applications which yield rapidly changing analog data. Such applications include studies of psychological conditioning, reactions to drugs, and autonomic responses to emotions and situations.

Studies in experimental psychology often require measurements of subjects' reactions to psychological stimuli. Where autonomic responses are being studied, the subject may be unable to describe or time the stimuli or to appraise objectively his responses, some of which he may not even be aware of. Recording several simultaneously occurring and sometimes rapidly changing reactions has been one of the technical problems in the study of autonomic reactions. Medical instrumentation has provided transducers to measure autonomic conditions of the human body, but a means of recording the data for later study and tabulation has been needed.

Use of a polygraph, such as a "lie detector," has filled the recording need in some cases. This instrument records body responses to each of a series of stimuli (questions put to the subject) as measurements inked directly onto a moving roll of graph paper. Ideal for inspection of the responses of individuals, the tabulation of these data to meet research requirements could be accomplished by a computer, but the raw data supplied by the transducers would have to be put in digital form for computer use.

The converter-recorder method was developed to record, for later statistical treatment, psychological data (subject reactions to visual stimuli given at 30-second intervals) acquired on a production-line basis. It scans the continuously measuring transducers at a 0.1-second repetition rate; since successive converted readings for any analog channel show little change they are, in effect, continuously presented measurements. The record for each stimulus consists of measurements during the 20-second post-stimulus period, which are compared against the baseline supplied by measurements of the same conditions during the 10-second pre-stimulus period.

Analog Data Handling

The converter-recorder will handle eight channels of analog measurements and two channels of pulse-coded session and time identification data. The following physiological conditions are measured by the transducers used: Skin resistance, respiratory movements of the chest, respiratory movements of the diaphragm, integrated muscle action potential, time interval between R-spikes of an electrocardiogram, pulse amplitude, skin temperature, and integrated shifts of body weight.

The analog signal in each channel is amplified by a preamplifier selected or designed for signals having the characteristics of that analog measurement. Six of the analog signals are also presented continuously on a strip-chart recorder for on-the-spot observations and initial equipment adjustments.

Conversion and Digital Recording

Both analog data and the digital session and time data are scanned by the converter at a 10 millisecond-per-channel rate to convert each analog channel to an 11-bit binary-coded digital signal. The 11 bits of digital information for each analog channel can accommodate integral numbers from -1024 to +1024 for a zero-centered range, for example. The digital signals obtained are buffered and again converted, this time to a maximum of five words of 36 binary digits each; this information is supplied to a diode selector matrix via 180 leads.

The diode selector matrix functions to connect successive groups of six digital lines to the six parallel heads which record the digital

signals on magnetic tape. The matrix has a format of five words, each with six characters of six bits each; it is scanned at a character rate of 300 cps to attain a word rate of 10 per second.

The six channels of information plus one channel for parity check are recorded on half-inch tape driven continuously at 1.5 inches per second. The tape transport used accommodates 10-inch reels for recording 12, 1/2 hour experiment sessions – a full word day.

The seven-channel recorded tape is the end-product of the data converter-recorder; the information recorded on it is ready for use by a digital computer. In its preparation, the presence of an operator is required only for initial checkout of the equipment, selection of the film strip which serves as the stimulus, and attachment of the transducers to successive subjects. The treatment of these data by a digital computer can eliminate all repetitive manual computation and minimize steps needed for statistical analysis.

Analog-to-digital converters and digital recorders are used for a variety of projects, especially where statistical treatment of the data is to follow. The present converter-recorder will be useful for recording several simultaneous channels of continuously read analog data, or mixed continuous and discretely quantized information (analog and digital), provided only that the reading repetition rate is compatible with the greatest rate of variable change. The 6-hour duration of a single reel of magnetic tape makes it particularly convenient to record and store a day's measurements.

NEW COMPUTING SYSTEMS—ORDNANCE TANK AUTOMOTIVE COMMAND, DETROIT 9, MICHIGAN

The Ordnance Tank Automotive Command (OTAC) has pressed the start button on OTAC's second generation electronic computer system. This action put computers to work for two new agencies using a Department of Defense-wide system and on eight new OTAC jobs. The new equipment, RCA 501 and 301 systems, will be capable of doing twice the work of the old computer at two-thirds the cost.

The new computer system will:

1. Control the Mobility Command's projected annual program of about $2.5 billion.

2. Be used in the Defense Automotive Supply Center's (DASC) annual program of about $200 million.

3. Prepare the procurement package to be sent to bidders and make preliminary bid evaluation.

4. Keep industrial readiness records and data necessary to buy approximately 1200 tank-automotive items monthly.

5. Analyze vehicle performance on the 1 million OTAC vehicles in the field.

6. Analyze internal cost and keep track of cost and deliveries on contracts.

7. Expand OTAC's computer system to provide support to DASC to supply manage 184,000 supply items, such as engines, tires, tubes, etc. – an inventory valued in the neighborhood of $800 million.

8. Fill approximately 3500 supply requisitions daily from Army, Air Force, Navy, Marines, and MAP countries.

9. Reduce processing time on high priority requisitions from 3 days to within 2 hours of receipt.

10. Print Supply Catalogs for the 256,000 Automotive Supply Center items.

11. Prepare $46,000,000 annual payroll for 6500 people.

12. Keep personnel records on 6500 people, including operation of the promotion program.

The new Mobility Command (MOCOM) will be composed of eight major field installations, including OTAC/Detroit Arsenal, operated by a total of over 12,000 military and civilian personnel. MOCOM will manage the whole spectrum of mobility equipment from research and development through production of over 238,000 separate items – well over half of all the items of the Army Materiel Command as a whole.

The Automatic Data Processing System (ADPS) in OTAC Headquarters will tie together the MOCOM program to be carried out in the following field installations;

1. OTAC/Detroit Arsenal, with 5226 personnel, and its responsibility for development, production, and procurement of tank-automotive

equipment, including tanks, self-propelled artillery, personnel carriers, trucks, trailers, and commercial vehicles for the Department of Defense.

2. General Supplies and Supply Control Offices, in Columbus, Ohio, with 328 personnel, is the National Inventory Control Point and National Maintenance Point for general supplies-type equipment, including materials handling equipment repair parts.

3. General Supplies Procurement Office, Columbus, Ohio, staffed with 194 personnel, procures general supplies-type equipment.

4. Engineer Maintenance Center, Columbus, Ohio, with 1117 personnel, is the National Maintenance Point for engineering equipment-construction machinery and electric power generating equipment. The Center is also the National Inventory Control Point and Stock Control Center for repair parts support for assigned items.

5. Engineer Supply Control Office, St. Louis, Missouri, with 795 personnel, is the National Inventory Control Point and Stock Control Center for engineering equipment, including construction machinery and electrical power generating equipment.

6. Engineer Procurement Office, Chicago, Illinois, with 280 personnel, procures engineering equipment, administers contracts, and is responsible for technical surveillance of contract specifications.

7. Aeronautical Agency and the Surface Transportation Agency, St. Louis, Missouri, are staffed by a total of 2218 personnel, with small elements in the Transportation Research and Development Office at Fort Eustis, Virginia, and the Aero Test Laboratory at Fort Rucker, Alabama. The Aeronautical Agency is responsible for procurement, inventory control, and maintenance for all aeronautical equipment, including observation, utility, and transport aircraft. The Surface Transportation Agency manages the procurement, inventory, and maintenance of amphibian, rail, marine craft, and overland trains.

8. Engineer Research and Development Laboratory, Fort Belvoir, Virginia, with 1775 personnel has the responsibility for research, design, development, and product engineering for construction machinery, electrical power generating equipment, and related items.

The analysis of vehicle performance will provide feedback data to research and engineering elements to isolate design problem; industrial elements to improve production and procurement through isolation of production, inspection, and/or testing problems; supply elements to isolate maintenance problems, determine feasibility of maintenance versus replacement, and analyze economies of maintenance. The data will be used to project probability studies to create new shapes and characteristics for vehicles. For example, based on these data, a determination might be made to change design and production characteristics to allow a 20,000-mile experience before major maintenance is required.

An example would be the analysis of certain type of springs on certain types of terrain. For example, desert terrain might result in such poor performance that a decision to use a different type of material might be made. This historical data can be used to establish new ground rules. OTAC might decide to build a spring for this terrain with the probability of going 15,000 miles before requiring any kind of maintenance. Computer simulation of performance before production will permit the design to get into production much more rapidly than possible with design models and tests. This technique will save time from design to use and will permit more accurate initial design.

The new computer system performs the following Supply Actions:

Determines customer priority

Checks availability

Checks location

Reduces balances

Records inventory

Flags danger levels

Redistributes stocks to depots (leveling)

Triggers procurement action

Controls procurement deliveries and dollars

Produces shipping instructions

Publishes changes to Armed Forces users

Establishes supply needs

Prices all actions.

The first generation, the RCA BIZMAC 1, used since 1956 to manage OTAC's 80,000 item

inventory, saved the government millions of dollars by eliminating duplicate requisitions and speeding supplies to the troops. It enabled Ordnance Tank-Automotive Command, never before able to fill Army Requisitions in the required three days, to process 95 percent of the requisition on time.

The new system will save even more because it will extend the area of use. In addition, prorating the initial cost of BIZMAC over the years of operation at OTAC and the annual maintenance figure, the cost to the government averaged more than $1.5 million a year. The new equipment will do twice the work of the old system at two-thirds the cost.

MATHEMATICS DEPARTMENT—U.S. NAVAL ORDNANCE LABORATORY, WHITE OAK, SILVER SPRING, MARYLAND

On the last working day of December 1961, an IBM 7090 was turned over to the Mathematics Department at NOL. This machine replaces an IBM 704 which had been in use at NOL for over 3 years. The computer configuration includes eight magnetic tape units (one switched over from the 1401 system) and the cathode-ray tube output unit which had previously been installed on the 704. The transition was smooth since most of the workload had been converted to the new system before its installation.

Since the installation, two changes in the computer configuration are contemplated. First, three additional tape units will be installed on the 7090 and one additional unit will be installed on the 1401 system. The reason for this is that many of the larger problems are being penalized by the small number of magnetic tape units. Compile and run has not been possible and full advantage of the simultaneous input-output could not be appreciated. These units are expected to be installed in June 1962. Second, the cathode-ray tube will be removed due to the high cost and low utilization of this unit. It is planned to handle the plotting load on other plotters in the Laboratory and by renting small amounts of time from other installations. The crt unit is due to be discontinued in June 1962.

ANALYSIS BRANCH—U.S. NAVAL UNDERWATER ORDNANCE STATION, NEWPORT, R. I.

The IBM 650, until recently the workhorse of the computing section, has been replaced by an IBM 1620. The system presently in use is composed of the central processor with floating point, card input-output, and 60K positions of core storage. The computer is used primarily for scientific computing in support of the R&D groups, and for processing data relating to weapons testing. Magnetic tape units will be added (September 1962) primarily to serve as information storage for propulsion test data. The present computer is being operated on a full one-shift basis. Off line peripheral equipment includes a full assortment of keypunches, sorters, 407, etc., as well as an oscillograph reader, film reader, and an electro-plotter.

Assistance to other naval activities in the Narragansett Bay area is provided, as required, on an overtime basis.

COMPUTATION CENTER—U.S. NAVAL WEAPONS LABORATORY, DAHLGREN, VIRGINIA

Stretch

A site is now being prepared for installation of an IBM STRETCH computer in late summer 1962. The system will include 48K core memory, a disc file, and 10 tape units. The STRETCH replaces an IBM 7090 which has been moved to another building for use, along with an additional 7090, in the Naval Space Surveillance system. Operation of the NORC will be continued.

It is expected that STRETCH time will be available for use by other government agencies and government contractors. Inquiries for such use should be directed to Head, Computation Division, Naval Weapons Laboratory.

High-Speed CRT Printer

The high-speed printer mentioned as under construction in a previous issue of this Newsletter, is now in regular operation. Connected to an IBM 1401, this printer records on 35-mm film the data from output tapes of a 7090, STRETCH, etc. Output may consist of alphanumeric characters or plotted point graphs; format is controlled completely by the tape and/or the 1401 program. Printing speeds up to 16,000 characters per second are attained. Hard copy is reproduced from the film by means of a Zerox Copyflow machine.

FLAME PROGRAM—U.S. NAVY DAVID TAYLOR MODEL BASIN, WASHINGTON 25, D. C.

FLAME, a flexible, three-spatial-dimensional, few-energy group (up to 4), nuclear reactor depletion code has been programmed for LARC at the Applied Mathematics Laboratory of the David Taylor Model Basin. The need for such a code to assist in the prediction of the life-time behavior of water-moderated reactors has been outlined by E. M. Gelbard, G. J. Habetler, and R. Ehrlich in the Proc. 2nd U. N. International Conference on the Peaceful Uses of Atomic Energy 16 (1958). FLAME solves a finite-difference approximation to the few-group neutron diffusion equations, taking account of interface and boundary conditions. As many as 100,000 network points can be treated. FLAME is the first practical program for treating problems of this magnitude.

PERFORMANCE DATA FOR LARC SYSTEM—U.S. NAVY DAVID TAYLOR MODEL BASIN, WASHINGTON 25, D. C.

The LARC System was turned over to the Applied Mathematics Laboratory, David Taylor Model Basin, for operation in February 1961. Reliability testing was completed successfully in September 1961. Table I lists performance data for the year June 1961 to May 1962.

When the system was turned over, the poorest reliability was experienced in the core memory and drum file sections. Performance totals for the drums tabulated in Table II show significant improvement over the first 15 months of operation.

Table I. LARC II Monthly Performance Figures

Month	Total ON Time	Productive Time	Down Time	Total No. of Interruptions	Mean Error Free Time	Down Time Per Error	Performance Percentage
Jun 61	466:30	293:24	32:16	85	2:43	:23	87.8%
Jul 61	471:00	336:16	69:04	151	2:13	:27	83.0%
Aug 61	556:00	383:05	112:02	186	2:05	:36	77.4%
Sep 61	456:00	368:47	27:54	86	4:18	:19	93.0%
Oct 61	309:02	217:05	15:08	37	5:51	:24	93.5%
Nov 61	332:20	243:42	15:09	37	6:35	:24	94.2%
Dec 61	330:23	223:47	35:41	50	4:28	:43	86.2%
Jan 62	352:53	249:32	43:06	79	3:10	:33	85.3%
Feb 62	414:05	357:31	23:49	64	5:35	:22	93.7%
Mar 62	514:50	429:04	37:18	61	7:02	:37	92.0%
Apr 62	454:29	383:07	21:44	73	5:15	:18	94.6%
May 62	411:06	311:18	29:14	86	3:37	:20	91.9%
Yearly Totals	5069:18	3736:36	462:18	995	3:45	:28	89.0%

Table II

3-Month Period	Drum Down Time	Repair Time per Failure
March to May 1961	383:25	10:05
June to August 1961	162:20	3:20
Sept. to Nov. 1961	53:45	2:15
Dec. 1961 to Feb. 1962	30:10	1:15
March to May 1962	15:10	:45

A comparison of the last two columns of Table II implies that the number of drum failures has remained fairly constant. Most of the improvement has been due to the less catastrophic nature of the failures and increasing skill of maintenance personnel in returning the drums to operation quickly.

Tables I and II cannot be compared directly, that is, the effect of drum failures on the overall system operation cannot be obtained from Table II, because of differences in measurement. For example:

$$\left(\begin{matrix}\text{Performance}\\ \text{Percentage}\end{matrix}\right) = \left(\begin{matrix}\text{Total time LARC was available}\\ \text{to run scheduled programs}\end{matrix}\right)$$

$$\left(\begin{matrix}\text{Total time}\\ \text{schedules for}\\ \text{programs}\end{matrix}\right) \times 100\% = \frac{\text{Productive Time}}{\text{Productive + Down Time}}$$

In this calculation, Down Time refers to time when the scheduled program cannot run. Table II lists all Drum Down Time, that is, all time charged against any drum in the system regardless of whether a scheduled program can run without it. Since most programs make use of only a few drums during the check-out phase, the total drum down time does not necessarily appear in system totals. With large scale full-capacity production runs such as FLAME, the entire system is used and all Down Time is significant.

COMPUTERS AND CENTERS, OVERSEAS

SIEMENS 2002—INSTITUT FÜR ANGEWANDTE MATHEMATIK, JOHANNES GUTENBERG-UNIVERSITÄT, MAINZ, GERMANY

Three IBM 727 magnetic tape units and a 10,000-word magnetic core storage were added to the Siemens 2002 (see DCN, April 1959) transistorized digital computer at this institute. The Siemens 2002 in the form which is installed here now includes a 12,000-word magnetic core storage and a 10,000-word magnetic drum.

LEO III TIME-SHARING—LEO COMPUTERS LTD., LONDON, ENGLAND

LEO III serial number 1 (see DCN, October 1960) has been installed at the Company Headquarters and number 2 has just been sent to South Africa to undertake work in association with Rand Mines. Fourteen of these medium size computers in the 150,000-350,000 area have been sold before the first one came on stream. This represents quite a success in England.

A problem that often faces the computer user in organising commerical jobs is that the data and results are large in volume, but that the Arithmetic Unit is not fully occupied by the input-output processes themselves. At other times the reverse may be the case, and the amount of calculating time required to do a job may far exceed the input-output requirements. LEO III enables jobs of these two types to be run on the machine simultaneously so that a far better balance is achieved between the reading of data, printing of results, and the carrying out of various calculations. The advantages of the LEO III system lies in the fact that the jobs are loaded and unloaded by the operators quite independently of one another and the programmer need only concern himself with the individual job that he is writing. Any set of jobs can be run together provided that there is sufficient peripheral equipment and storage available. The grouping is thus at the discretion of the operator on the spot.

Automatic Interruption and the Master Routine

The key to the LEO III system is the method of automatic interruption used to cause a switch between the various programmes operating at the same time. This efficiently provides a means of time-sharing. However, time-sharing is a system concept, not just a matter of hardware, and LEO has supplemented its machine interruption feature with an extensive operating and programming method which actually simplifies the work of the programmer and allows both operator and programmer to treat each programme as a completely self-contained entity. LEO deliberately allotted a separate development group to the project of preparing this software, because it was seen that without it the full advantages of the computer facilities offered would not be achieved by the user.

The main elements of the software are the translator which interprets the programmers coding (Intercode) into machine language coding and the Master Routine.

The Master Routine lists the programmes running in an order of priority. Whenever a high priority programme cannot continue because an item of equipment is engaged, the priority control section of the Master Routine causes control to be passed to the next programme in the priority list. When an item of equipment which caused a delay becomes free it signals the fact, automatic interruption occurs, and priority control takes over and locates the top priority programme now free to continue.

Special Checks and Precautions

Various precautions have been taken to ensure that the parallel operation of programmes does not result in any errors which would not otherwise occur. On the programming side, all the necessary features, such as tests or equipment readiness, are automatically incorporated by the autocode translation routine; loading of the programme and allocation of store space is checked and executed under the control of the appropriate sections of the Master Routine. This ensures that a programme is not loaded unless the necessary equipment and storage is free and so guarantees that there is no conflict between programmes.

The Tag Reservation System

As a further precaution against one programme altering the data or instructions appertaining to another programme, the LEO Tag Reservation System enables each word in the computer store to be marked with a tag identifying its allotted programme. If a programme attempts to refer to a location outside its own store area, a special interruption takes place and the programme is suspended. The same feature is used to prevent input-output equipment from overrunning the buffer areas of storage to which they are required to work.

The Demonstration

The object of the demonstration is to show three programmes running together on a time-sharing basis, as follows:

Programme A. Magnetic Tape to Printer

Programme B. Paper Tape to Magnetic Tape including a sequencing routine

Programme C. Counting Programme.

These programmes will run in the above order of priority with A taking precedence.

The volume of data for each programme has been so adjusted that each will run for approximately the same length of time when run together.

Each programme will be firstly run by itself, then followed by a simultaneous operation.

A comparison of the times for programmes running separately and all three run together follows. The left-hand column, "% ACT" refers to the degree of activity of calculating unit of the computer, expressed as a percentage of the total running time for the programme.

Table I

% ACT	Running Alone	Time Shared	
		Theoretical	Recorded
A 12	6 min 41 sec	6 min 45 sec	6 min 41 sec
B 75	7 min 19 sec	7 min 37 sec	7 min 28 sec
C 100	2 min 30 sec	9 min 6 sec	8 min 38 sec

The theoretical running time has been calculated by taking into consideration delays caused by other programmes sharing input and output channels or the calculating unit. These calculations are approximate and the actual figures quoted above depend on the skill with which individual operators carried out the various runs.

When all three programmes are running together, the running efficiencies of Programmes A, B, and C are calculated to be 99, 96, and 12 percent, respectively.

On completion of Programme A, Programmes B and C continue and their theoretical running efficiencies are calculated to be 99* and 24 percent, respectively.

From these figures, when time is shared the theoretical running times are calculated to be those shown in Table I.

*The top priority programme does not necessarily operate at 100-percent efficiency because there is a very small overhead of time spent by the Master Routine in carrying out its supervision functions.

LEO III/F—LEO COMPUTERS, LTD., LONDON, ENGLAND

LEO III (see LEO III Time-Sharing, this issue DCN) has been designed as a general purpose computer for application to a wide range of business problems. It has been built on the modular principle with the main frame, individual blocks of storage, and input and output channels all physically separate, so that a wide range of different assemblages can be formed to suit different needs incorporating standard parts.

Experience has already demonstrated that LEO III is admirably suited to the needs of a wide range of organisations. However, for users who have very large volumes of work involving lengthly calculations or calling for simultaneous execution of several jobs, a LEO III/F can be provided with faster arithmetic circuits and a store with quicker access elements. The latter can have a store cycle time of 2.5 or 6 microseconds according to need. The resulting overall speed of arithmetic operations is respectively 3 or 5 times that for the standard model.

To ease the engineering problems of working at the higher speeds, the design of the equipment is more compact and has resulted in a reduction of two cabinets for housing the main frame. As is to be expected however, the cost of the faster circuitry is greater than for the standard computer; for example, for a store of 4096 long words with cycle time of 6 microseconds the main frame will cost about 25 percent more.

The logical design of LEO III/F is fully consistent with that of the now standard system, inasmuch as completely standard assemblers are used. Any new assemblers which may be announced later for the standard model will be suitable for the faster one and vice versa. The instruction code is the same as that of the standard LEO III. Full programme compatibility is thus assured.

As in the standard model, both mixed radix and binary arithmetic are provided. Floating-point arithmetic in binary is fitted to all LEO III/F models.

The equipment is planned to be available early in 1964.

LEO DOCUMENT READER—LEO COMPUTERS, LTD., LONDON ENGLAND

The LEO Document Reader is a relatively simple and cheap machine for the automatic reading of handmarked documents.

Many suggestions have been made for the automatic reading of data recorded by cash registers, adding machines, and the like, as recognisable printed characters or as holes punched in paper tape or cards. Such recording equipment is relatively expensive, and so are reading machines for printed or typed characters. So far there are no machines available for reading handwritten characters.

We feel that in many cases it is desirable to be able to produce an automatically readable document simply by means of a pen or a pencil, without any expensive or cumbersome equipment. This would enable, for instance, a salesman in the field to take orders without having to carry around with him a portable typewriter or punch. Generally, it is more convenient and also cheaper to use a pencil or a ball-pen instead of a typewriter or an adding machine. Such a handmarked document subsequently can be read directly into a computer.

Investigation of various data preparation jobs leads us to believe that documents properly designed for handmarking can be most effective, and that in many cases handmarking can be just as easy and convenient as handwriting, sometimes even more so. Suitably designed handmarked documents are easier to read automatically than typed characters, and a machine for reading marks can be produced more cheaply than a character reader.

The LEO Document Reader has been designed for a specific application, namely the ordering and dispatching of bakery products for a considerable number of retail shops. However, it can read a great variety of different forms, provided they are of a suitable size and have the specified arrangement of columns and rows. A typical form is shown in Fig. 1; the marking is done simply by drawing a line connecting the two dots of the required square. Ball pen or pencil (preferably grade HB or B) may be used. A form may have up to 16 vertical columns and up to 99 horizontal rows of squares, the significance of each column and row being clearly designated.

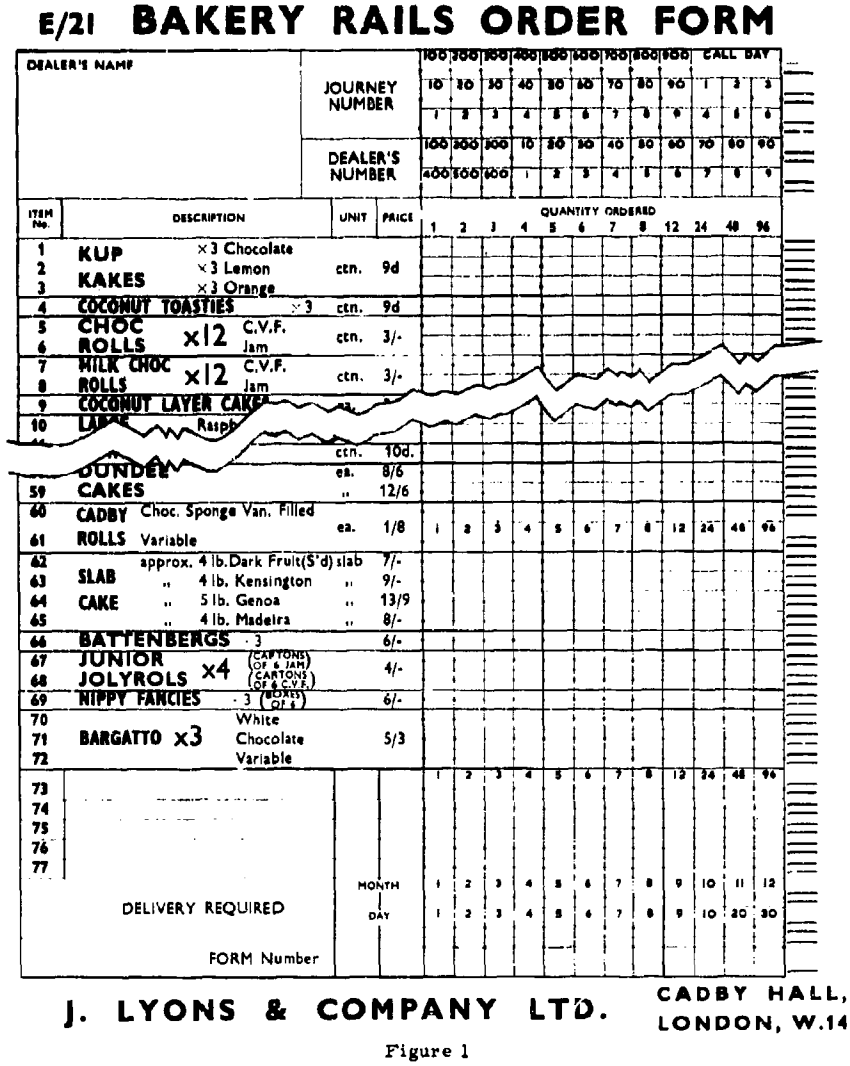

Figure 1

Columns are spaced four to an inch; minimum row spacing is six to an inch. Forms may be from 5 to 10 inches wide and from 4 to 18 inches long.

Pairs of horizontal lines at the right-hand end of each row are location marks which define the scanning period for each row. The mark drawn between two dots in a square must be sufficiently straight to remain within the two location lines. If it is desired to erase a mark, it is sufficient to smudge it so that it fills the top half of the square, or at least extends beyond the upper location line. This method is effective because the signal results from the boundary between light and dark rather than from the centre of the dark area.

Handmarked documents tend to become dirty. While a proper mark produces an amplified output of the reading photocell of more than 20v, a smudge or fingerprint may produce

up to 15v. Similarly, a weak mark may produce something like 15v. To cope with such border cases we introduced the concept of a doubtful mark. When a doubtful mark occurs, that is when the output of any reading cell is about 15v, the machine stops, and an alarm light on the control panel indicates the respective column. The operator then examines the line of marks being scanned through a veiwing window, decides whether the doubtful mark is valid or merely a smudge, and restarts the machine by pressing one of two buttons either to accept the mark or to ignore the smudge. However, in order to speed up the procedure we are going to change this arrangement. In future the row in which a doubtful mark occurs will be automatically marked and the form ejected into a reject box without stopping the machine.

At present our Document Reader is coupled to a tape punch, so that the information scanned from the document is punched into tape. However, it is possible to provide a facility to punch the information into cards, or to feed it directly into the computer.

At present the documents are fed through the Reader at a speed of 20 inches per second. Each time a mark has been sensed the paper stops and punching commences. Using a 110 characters a second Teletype punch, the punching of each line takes about 60 msecs. Actually for each marked line on the form we punch on the tape three rows of information, two rows for the line number, and the NUMBER END indication. For a foolscap form with 15 lines marked, the total time taken for reading and punching is about 2-1/2 seconds, or approximately 1440 forms per hour. This is approximately 32 times faster than handpunching and verifying.

The end of the form is sensed by the machine as a wider gap between the last two location marks. The Document Reader then punches a BLOCK END character followed by five blank rows. This blank space helps the visual identification of forms on the paper tape.

When the end of form signal is detected, the number of lines counted is compared with a preset number. In case of disagreement the form is ejected, and the machine punches five rows of all holes, five rows of blank tape and a BLOCK END character.

The proper functioning of all reading photocells is automatically checked after the passage of each form.

The experimental Document Reader was used for a 6-month trial run on orders actually taken by travellers. Following this, it read documents continuously for 2 days. Out of many thousands of marks on the documents 0.3 percent gave doubtful mark alarm. Not a single mark was missed.

On the basis of this experimental machine an improved version has been designed and made as a pre-prototype machine. Production machines are expected to be available towards the end of 1962.

The LEO Document Reader is merely an optical mark-sensing machine; it is not a character reader. We make no apologies, because we are sure that our machine does help in many cases to solve the problem of data preparation.

Further developments of our Document Reader are directed towards speeding-up, direct use on-line, recognition of printed marks produced on a high-speed printer, improvement of marking accuracy, and the use of continuous stationery.

AN ARTIFICIAL LANGUAGE FOR INFORMATION RETRIEVAL—NATIONAL PHYSICAL LABORATORY, AUTONOMICS DIVISION, TEDDINGTON, MIDDLESEX, ENGLAND

The ACE computer is being programmed in an experiment to construct an artificial language to be used for the indexing and retrieval of information. This artificial language will consist of overlapping groups of statistically related key words. A many-one transformation will map statements in natural language on to corresponding statements in the artificial language. It is hoped that, in this way, sets of statements in natural language that would normally be regarded as being equivalent (e.g., differently worded requests for information on a given topic) will be mapped on to the same statement in the artificial language.

The ACE program will analyse a large quantity of scientific text and obtain the frequencies of occurrence of keywords and of pairs of words occurring within the same context. By applying a test of statistical significance (e.g., chi-squared test) the statistically related pairs of words will be found. The keywords will then be grouped in various ways on the basis of this information. The word groupings thus obtained will then be evaluated and compared by using them in an experimental indexing and retrieval system.

High-Speed Computing

The work of the High-Speed Computing Group of the Autonomics Division has been concentrated on a study of the potentialities of the thin film cryotrons formed by vacuum deposition.

Studies of thin films of tin have shown that both the superconductive properties and the crystalline structure are strongly dependent upon the conditions of formation of the film. It is of particular importance to reduce the partial pressures of oxygen, water vapour, and carbon dioxide during deposition. Close control of the substrate temperature and the rates of vapour deposition are also essential.

Simple cryotron circuits of tin, lead, and silicon monoxide insulator have been tested and their time constants have been found to agree with those predicted from a knowledge of cryotron normal resistance and circuit inductance. It should be possible to reduce the circuit time-constants by a factor of 10 when a really reliable thin film insulator is found which will stand repeated thermal cycling.

The next stage in the work is the making and testing of more complicated circuits such as shift registers. The liquid helium cryostat already in use will hold at least 20 substrates each 4 inches square. Impedance matched interplane connections will also be studied.

Character Recognition

Work is being carried out on a multi-font reading system based upon a feature description of a character. An auto-correlation process is used to detect the orientation, length and position within the character, of straight lines and curves. The use of auto-correlation permits detection of these properties independent of the position and orientation of the character. The range of application of the approach is being investigated with an optical system using photographed copy in transparency form. The principal problem here involves the choice of a small number of auto-correlation functions which adequately described the characters to be recognised.

The need to evaluate any specified auto-correlation function for an opaque pattern, has led to the construction of a prototype reading device. This consists of a flying spot scanner feeding analogue networks which compute a restricted class of auto-correlation function. It is expected to read any single style of numeral at a high speed.

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MISCELLANEOUS

MULTI-FONT CHARACTER RECOGNITION—CORNELL AERONAUTICAL LABORATORY, INC., BUFFALO, NEW YORK

During the past 6 years Cornell Aeronautical Laboratory (CAL) has been engaged in a continuing program of pattern recognition research. Recently a portion of this work, supported by the Office of Naval Research, has turned toward the application of the perceptron class of pattern recognition devices to such useful tasks as the recognition of printed characters in machine scanning of business reports or tax forms. The overall program is based on numerous pattern recognition systems and concepts, including those derived from the early perceptron work.

Objective: Recognition of Imperfect, Mixed-Font Characters

The objective of CAL's current program is to investigate computer concepts for recognizing imperfect printed characters of varying type faces, i.e., mixed fonts. Supplementing analytical studies, a highly flexible general-purpose computer implementation of a recognition system is employed. This research was stimulated by earlier experiments with the Mark I perceptron, which demonstrated the ability of such a unit to recognize a complete alphabet with a limited amount of distortion. The same machine was used to establish the fact that recognition of limited sets of the alphabet could be accomplished, with proper

training, using a large amount of distortion, translation, and noise

To illustrate multi-font characters, Fig. 1 shows the first seven letters of the alphabet in both lower and upper case in three of the fonts used in recent studies. Upper-case letters are recognized as distinct from lower-case letters, since there may be significant information content in the fact that a letter is upper or lower case. Figure 1 illustrates the marked geometric differences in the three fonts selected. The first font, taken from a Buffalo newspaper, is a bold type using a minimum of serifs or detail. The second font, which was taken from a second local newspaper, is an italicized type with serifs and more detail incorporated. The third font contains the well-known addressograph characteristics. To get these undistorted letter samples, considerable retouching had to be done to eliminate a large amount of noise and distortion inherent in the available samples. The formation of the lower case "a" in the three fonts is markedly different, with the second font incorporating no upper loop in the formation of the italic "a." Throughout the alphabet, similar variations from one font to another can be observed.

The types of noise and distortion incorporated in the samples as part of this program are illustrated in Fig. 2, which shows typical imperfect characters in the three fonts. In some cases the distortion is that of background noise produced by the paper; in other cases the noise is that of geometric distortions of the character produced by the method of making the impression.

a b c d e f g

a b c d e f g

a b c d e f g

A B C D E F G

A B C D E F G

A B C D E F G

Fig. 1

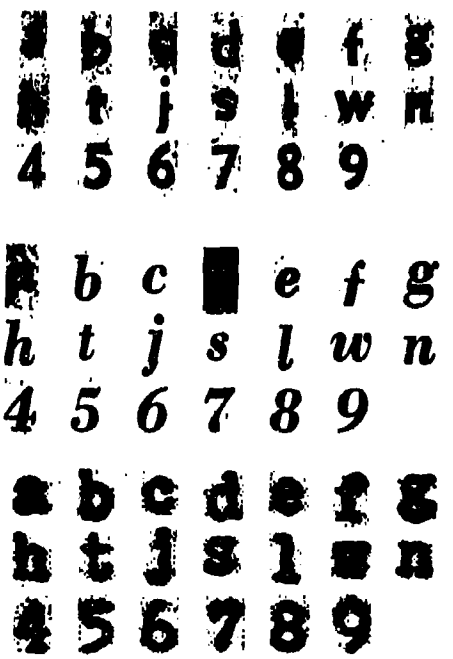


Fig. 2

Experimental Facilities

Since it was intended to implement pattern recognition devices in a general-purpose computer (IBM 704), a means of inserting pictorial material into that computer was necessary. For this purpose, the system shown in Fig. 3 was constructed. The output of a commercially available facsimile machine was converted to digital form for insertion into the real-time package of the 704. The facsimile machine was modified to provide special synchronizing signals used by the control system to coordinate reception of the 704 successive binary words representing image density. The result of processing an undistorted lower case "a" from one of the type fonts into the 704 is shown in Fig. 4. The figure is the result of making a printed readout from the tape memory of the stimulus in the machine. Although the input system produces 16 gray scale levels in the 704 from photographic material, the output in this case has been thresholded to produce a binary output.

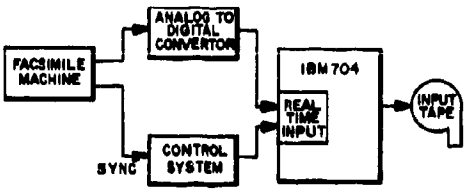


Fig. 3

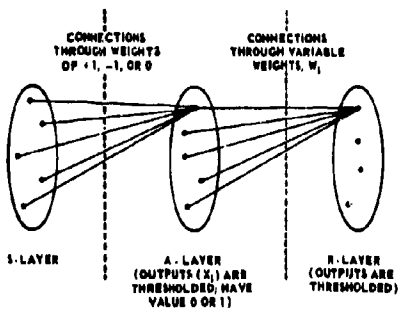


Fig. 4

Procedure for Establishing Initial Weights

Normally it is not known at the outset what the variable weights should be. Several training routines were proposed and used in the original perception research. They have been shown theoretically to converge to a solution (correct classification) if a solution exists. As the number of different patterns in the 0 and 1 classes and the number of dichotomies which must be achieved increase, the training time can become rather long.

For example, to recognize uniquely all the upper case and lower case letters together with the numerals and a reasonable set of punctuation marks, it would be necessary to expose the machine in training to over 70 symbols, requiring many exposures per letter during the training. To reduce training time a method for initially setting the weights, based on the use of Bayes' theorem,* was hypothesized. It was necessary to employ some assumptions to make these initial weight selections: (1) use Bayes' rule, and (2) assume that the A-unit outputs are statistically independent. Since the second assumption is not completely valid, the initial weight selection is not expected to be perfect. However, these assumptions do provide a means of shortening the training cycle, and expeditiously deriving the weights necessary to the design of a practical machine to recognize printed characters.

*Classification based on probability densities and prior probabilities.

First Results

A 100-A-unit perception has been trained to recognize six undistorted letters of the alphabet in both upper and lower case versions and in three fonts. In doing so, it was distinguishing each of the 12 distinct symbols from all fonts, upper and lower case, as well as all numerals. The significance of accomplishing this in a 100-A-unit machine can be appreciated by the following observation: although very few experts doubt the ability of perceptrons to perform difficult recognition tasks, many have feared that a perceptron, designed to recognize many fonts in many complete alphabets, and upper/lower cases, would be prohibitively large. The actual implementation of a 100-A-unit perceptron would be very moderate. In fact, the Mark I, which was built using elementary concepts without any prior experimental model on which to base the design, had 500-A-units.

The most exciting result of the initial experiments, however, was the finding that in every case (except one in which the threshold for the A-unit linear discriminator was placed too high) the initial weight selection produced a machine which required no further training. In other words, having gone through the Bayes' rule computation of weights for the 100-A-unit perceptron, the device properly classified all the undistorted examples presented to it. Thus, without any further training the machine gave a positive output for the desired positive class symbol, whereas exposure to every other letter of three font alphabets in both upper and lower cases and the 10 numerals, produced a negative output. This result was achieved with all 12 of the symbols to which the machine was trained. When the threshold for the A-units was made as high as three, however, four training cycles were required before completely correct classification was achieved. For thresholds of two and one, the machine accurately classified its input immediately after initial weight computation.

In subsequent tests an R-unit was trained to recognize undistorted lower case n's in several different positions in the input field. After this training, the machine was tested by having it

classify all of the letters and numerals in the distorted or noisy alphabets of the three type fonts.

The results were quite encouraging, in that only 28 mistakes occurred in the classification of 186 characters – a 15-percent error ratio. Of these, one was an incorrect classification of a noisy n, and 27 were cases in which other letters or numerals were classified as an n. This percentage is also higher because the system is not complete. In a complete system there would be an R-unit for each letter or numeral. Relative outputs of all R-units properly scaled, would be compared, with the highest positive output identifying each letter. Therefore, in a complete system, some of the 28 errors of mistaken letter identity would not have occurred because other R-units would have higher outputs than the output of lower case n's.

Future Experimentation

As mentioned earlier, this is a continuing program and the results reported are preliminary in nature. CAL plans to continue experiments exploring character noise and translation. In the course of this research, an increase is anticipated in the density of S- to A-unit connections from the 10 excitatory and 10 inhibitory connections employed in the initial experiments. The results of subsequent experiments should suggest variations on the main line of research. CAL expects to explore these variations.

HIGH-SPEED VIDEOGRAPH PRINTER-PLOTTER – A. B. DICK COMPANY, CHICAGO 48, ILLINOIS

A high-speed electrostatic printer which simultaneously prints a permanent paper record of both alphanumeric data and analog curves at speeds up to 10 inches per second has been introduced by A. B. Dick Company. It is believed to be the first printer-plotter with these capabilities.

The Model 9041 Videograph Printer-Plotter performs as an analog recorder, a digital page printer, or combines both forms of output. It operates on information received from a data acquisition system or from playback of magnetic tapes. Data is printed out directly on an 8-1/2-inch-wide paper web.

The Company also announced that the first production model of the printer-plotter has been purchased by the Rocketdyne Division of North American Aviation, Inc., along with an A. B. Dick Input Control System. The equipment will be used to record results of rocket engine testing.

In addition to its high speed capability, the major advantages of the printer-plotter are high reliability, flexibility, and low operating cost. With it, film processing and printed forms are eliminated.

Prints Through Cathode-Ray Tube

The printing function of the printer-plotter is performed through a special cathode-ray tube having a matrix of fine metal wires permanently sealed through its faceplate. The electron beam of the tube is deflected and modulated by means of video-type electrical signals across the inner ends of the wires, while the outer ends of the wires are in contact with a moving web of paper. The paper is coated with a simple dielectric material which received latent electrostatic images directly on the surface of the paper. These charge patterns are made visible and permanent through a developing process.

For alphanumeric printing, a special Videograph Character Generator is employed to convert digital input signals into waveforms that are directed to the matrix of the tube to form character-shaped images on the paper at high speeds.

Through suitable control circuitry, the electron beam of the tube can be directed in a linear sweep by video input signals or driven in response to digitally coded input signals for accurate point plotting.

3600 Lines Per Minute

As a page printer the unit prints out a format of 72 columns with ten characters per inch, five to seven lines per vertical inch, at a rate of 3600 lines per minute.

A manually operable cutting attachment permits selective cutting of the web into any output length. Output also may be rewound into roll form.

Only manual functions required for operation of the printer-plotter are replacement of the paper supply roll and charging and replenishment of the developer. Controls are push-button type, with indicator lights.

The unit is approximately 54 inches long, 24 inches wide, 42 inches high, and weighs 750 pounds.

Input System Design

Design of the input control system used with the Videograph Printer-Plotter depends on the specific application involved. The complete system designed by A. B. Dick Company for Rocketdyne has the function of producing continuous multiple curves or traces of test data obtained from a data acquisition system. In the data acquisition system, sensory instruments located at a test position will provide as many as 150 inputs of analog information to a data control center.

At the data control center, each of the analog inputs will be converted into a four-digit decimal number which will be transmitted in digital form to the printer-plotter output system for recording.

AUTO-CORRECTIVE OPTICAL SCANNER— HONEYWELL EDP DIVISION, WELLESLEY HILLS 81, MASSACHUSETTS

Honeywell Electronic Data Processing (EDP) has announced the development of an exclusive auto-corrective technique for use with its optical character readers that should reduce to 0.2 percent the document rejection rate because of mis-scanning or defaced information. Document rejection rates generally accepted by the EDP industry in scanning operations range from 5 to 10 percent.

Auto-correction is achieved in the Honeywell system through addition of two or more ortho-correction (checking) digits to the information on the document to be scanned. By means of these digits the scanner, linked to a Honeywell computer, automatically regenerates lost or damaged data. Documents remain readable to the scanner even though portions of the document containing the data have been defaced. The correction process is accomplished without interruption and without rejection of the document.

The technique represents a new, two-way approach to reliable optical scanning. The reading device has the ability to scan and re-scan any document any number of times, at high speed and without machine interruption. This compensates for temporary scanning failures – such failures as might be caused by a speck of dust on the document. The document acceptance rate, however, is even more substantially increased through the orthotronic regeneration of incorrect or permanently defaced data. The combination of orthotronic control and automatic re-scanning accelerates the input of data to the computer and effects a major improvement in the percentage of document batches automatically processed by the scanner without manual intervention.

Test runs of orthotronic scanning at Honeywell's EDP engineering laboratories were performed as follows:

Batches of some 250 documents were produced on a high-speed printer connected on-line to a Honeywell 800 Computer which calculated and appended the ortho-digits to the data to be scanned. (The printing of these ortho-digits requires no additional time.) The scanner, connected on-line to the trunk system of the Honeywell 800, processed the batches with the orthotronic control capability inoperative. The reject rate, after hundreds of runs, averaged about 8-15 percent, or 23 documents in each batch of 250 documents. In a conventional scanning system, each of these rejected documents would have had to be examined manually to determine the reason for the scanning failure. Re-scanning the same batches, with orthotronic correction, resulted in the document rejection rate dropping to 0.2 percent, which is less than one reject per batch.

Returnable Media

In the case of returnable media documents, such as invoices and subscription forms, the ability of the Honeywell computer to calculate and append the orthotronic digits to the data printed for scanning, provides "turn-around" documents to which no further information need be added for corrective purposes prior to optical reading. However, a "mark-scan" option is available with the Honeywell computers for use in instances where additional information is to be added to "turn-around" documents prior to scanning.

The Honeywell system is a breakthrough in optical scanning and is certain to have a marked impact on the future development and applications feasibility of document reading. In other scanning systems any document that cannot be read correctly, regardless of reason, is automatically rejected by the scanner. These rejects then require special handling.

Orthotronic-correction will be standard procedure with all Honeywell optical scanning systems, several of which are on order for delivery within the next few months.

THE M-2CR MEMISTOR—MEMISTOR CORPORATION, MOUNTAIN VIEW, CALIFORNIA

A new electronic circuit element called the memistor (a resistor with memory) is being manufactured in several forms by Memistor Corporation for use in adaptive systems, threshold logic systems, analog systems, and hybrid analog-digital systems. The Memistor consists of a conductive substrate with insulated connection leads, and a metallic anode, all in an electrolytic plating bath. The conductance of the element is reversibly controlled by electroplating. Like the transistor, the memistor is a three-terminal element. The conductance between two of the terminals is controlled by the time integral of the current in the third, rather than by its instantaneous value, as in the transistor. The memistor is functionally equivalent to a transistor with a "built-in" integrator.

The memistor was invented at Stanford University by B. Widrow and M. E. Hoff. Their original work was done under Tri-Service support, administered by the Office of Naval Research.

Adaptive "Neuron" Circuits

The memistor was developed to provide simple, cheap, and reliable variable-gain elements with memory for adaptive threshold logic circuits. The ADALINE "neuron" consists of an adjustable threshold function and the adaptation machinery for automatically adjusting its weights. (This is described in Stanford University Electronic Laboratories Technical Report 1553-1 of June 1960, by B. Widrow and M. E. Hoff.) The structure of ADALINE changes somewhat with each training experience. A steepest descent method requires that each of its weights be changed by the same magnitude with each training cycle, some weights increasing, and some decreasing, depending on the state of the input signals and the desired output state. The memistor allows a very natural implementation of such an adaptive process. A memistor cell stores a single weight in the value of its conductance. Current sources of fixed magnitude are turned on simultaneously to plate the memistors, and they are sensed by ac-voltage sources. Their current outputs are summed by a Kirchhoff adder. Information is stored in the memistorized ADALINE in terms of the thickness of plated metallic films.

Very complex logic functions can be trained into threshold elements and networks of threshold elements. These will provide adaptive logic, "neuron" memory systems with associative information storage and retrieval, pattern classification systems with generalizing capabilities, and reliable digital systems that can adapt around their own internal flaws. All of these characteristics and capabilities have been demonstrated, at Stanford with a machine called MADALINE which contains 300 memistors. MADALINE is currently being tested in a connection to an IBM 1620 computer.

Analog Circuits

Memistors have been used as integrators, multipliers, modulators, pulse counters, time base generators, and in sample and hold circuits. The inherent characteristics of the device, such as long-term stability, relative insensitivity to temperature, linear relation between conductance and integral of plating current, ability to integrate long pulses and extremely short pulses, low power requirements, and compact size and weight, make it attractive for analog applications.

M-2CR Memistor Characteristics

Memistor M-2CR can be plated over a resistance range from 30Ω to 2Ω, and covers this range in 10 seconds with a plating current of 0.2 ma. The plating potential is 0.2 volt, so the required plating power is 0.04 milliwatt. Sensing the conductance without destroying the stored information is accomplished with ac voltage that could range in frequency from 60 cycles to several megacycles. The integration of the plating current is accurate to within 5 percent, regardless of the frequency content of its waveforms. Pulses as short as 0.5 microsecond have been integrated.

The M-2CR cells are made in single units for analog applications, and in sheets of 10 or 20 for adaptive neuron applications. Those that are printed on sheets have had, at the same time, some of the resistors and interconnections of the ADALINE element also printed. This is a first step towards completely integrated neuron circuitry. Each memistor cell contains about two drops of plating fluid, and is encapsulated. The M-2CR is insensitive to shock and vibration, is non-microphonic, insensitive to temperature (taken from 100° to -196°C with no permanent change in characteristics), and exhibits less drift than 1 percent per week. As an electronic integrator, the time constant is of the order of several years.

At the present time, work is progressing toward making these cells more accurate as analog integrators (goal is 1 percent), making them faster with less power, making them more stable, and reducing costs in volume production to make large networks of adaptive neurons economically feasible. At the present time, a rough figure for a completed neuron system, almost regardless of configuration, is about 50 dollars per weight.

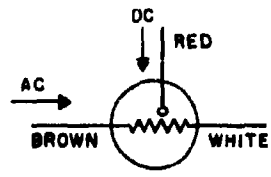


Fig. 1

Electrical Specifications

The unit is an electronically adjustable resistor with the rate of change of resistance controlled by dc-current in a third electrode. Over the active range of the memistor, the rate of change of conductance is proportional to the control electrode current, and is essentially independent of the resistance value. The resistance range of the memistor covers from 30 ohms to about 2 ohms (0.033 mho to 1/2 mho).

Three leads, brown, white, and red are provided (see Fig. 1). The resistance (of the substrate) is measured, using an ac-current, between the brown and white leads. The ac-voltage drop between these leads should not exceed 0.1-v rms.

To decrease the substrate resistance, the red lead is made positive with respect to the brown and white leads. The average dc-current into the red lead should not exceed 0.25 ma. The dc-voltage drop across the cell will be about 0.2 v. For a plating current of 0.2 ma, the rate of change of conductance is about 0.03 mho/sec (the resistance changes from 30Ω to 2Ω in 10 seconds).

The resistance of the substrate may be raised by making the red lead negative with respect to the brown and white leads. Again currents should not exceed 0.25 ma, and the rate of change of conductance is the same.

When the resistance of the substrate is set to its maximum value (completely stripped), a negative voltage connected to the red lead will produce relatively little plating current. The voltage drop across the cell should not be permitted to rise in excess of 1.5 v, or gas will be produced in the cell.

When this voltage is removed and the red lead again made positive, the resistance will begin to fall immediately. However, when current tending to reduce the resistance below its 1 ohm minimum is applied to the cell for a length of time, the current must be reversed and maintained for approximately the same length of time before the resistance will begin increasing.

PHOTOCHROMIC DYNAMIC DISPLAY— THE NATIONAL CASH REGISTER COMPANY, HAWTHORNE, CALIFORNIA

A contract for a photochromic dynamic display has been awarded to the Hawthorne, California electronics division of the National Cash Register Company by the Naval Ordnance Test Station at Pasadena, California.

The display will be used to analyze computer data display requirements in real-time applications for advanced Navy weapons systems.

The display provides real-time tracking through the use of slides coated with a molecular dispersion of light-sensitive, reversible photochromic dyes.

Tracks appear on the slide when individual molecules of the normally transparent dye are switched to an opaque state by beams of ultraviolet light moving in response to input signals. These tracks, as well as background reference information, are projected onto the display screen.

A unique feature of the display is that persistence of the opaque tracks can be varied by controlling illumination intensity, since high-intensity light returns the dyes to their transparent state. This property also allows the tracks to be easily erased.

The $65,000 contract covers the fabrication and installation of the display unit.

HOME-STUDY COURSE IN COMPUTER PROGRAMMING—PENN STATE AND IBM, UNIVERSITY PARK, PENNSYLVANIA

The Pennsylvania State University and International Business Machines Corporation announced what is believed to be the Nation's first university-sponsored home-study course in programming. The need for a course of this type is based on the extension of electronic data processing into almost every area of business, government, and science.

Many computer users, facing a shortage of programmers, have set up their own training programs; but it often is difficult for them to find qualified people to enter the training programs.

Students who complete this programming course with high grades will have indicated that they have the interest and aptitude required for this work.

What kind of aptitudes are required for programming?

A background in college mathematics is helpful; but a college background is considered less important than a keen analytical mind, capable of reducing complex problems to their component parts and perceiving the easiest, most direct solution.

IBM has prepared a 12-part textbook for the course. A home-study guide, which helps fill the role of the instructor, has been prepared by Penn State. It advises the student how to get the most out of the course.

The course covers the entire range of programming principles as they apply to all computers, from the smallest business computer to the most powerful scientific system.

It introduces the student to the basic elements of data processing; explains the equipment, and takes him into the coding of a program. In more advanced sections, it covers technical subjects such as symbolic programming, address modification, branching, and other operations.

The entire course is administered by mail. The teaching staff of the university supervises lessons and grades test papers. Final examinations are given by a proctor selected by the student in his home city.

Students receive a final grade an a completion certificate when they finish the course.

Tuition, including all costs of handling the course, testing, and administration, is $24. Cost of the text and mailing is approximately $10.

The programming course is the newest in a series of correspondence courses offered by Penn State in cooperation with IBM.

Among these are courses in punched card data processing principles and punched card applications. There are also courses in electricity and electronics with emphasis on computer applications.

Penn State has been giving correspondence courses, many for college credit, since 1912. Each year more than 10,000 home-study courses are given to an estimated 8000 students all over the world. A staff of 16 directs this complex operation.

SYMPOSIUM ON OPTICAL CHARACTER RECOGNITION—15-17 JANUARY 1962, WASHINGTON, D. C.

A Symposium on Optical Character Recognition, held 15-17 January 1962 at Washington, D. C. under the joint sponsorship of the Office of Naval Research (ONR) and the National Bureau of Standards (NBS), was attended by more than 300 computer scientists and users from the United States and abroad. Plans for the symposium were made by a conference committee consisting of Donald K. Pollock (ONR), Bernard Radak (BUSANDA), and Mary E. Stevens (NES). Twenty-two papers covering both the operative and research phases of optical character recognition systems were presented in two sessions. This was followed by panel discussions of (1) user requirements for new systems, and (2) the horizons of optical character recognition work.

Many experts believe that the next great step forward in automatic data processing will come through the development of techniques for automatic character recognition. Data processing systems in use today require, as inputs, information that has been carefully translated into the machine's language and encoded in a suitable medium. Only a few systems will accept information not already coded on cards or tape. One such system, FOSDIC, developed by NBS for the Bureau of the Census uses

optical sensing of response placement in a format designed to be self-coding. Another type of machine identifies documents by magnetically scanning areas of numerals printed in a specially designed typeface and with magnetic ink. Present-day devices, a few in operation and others under development, can read one or a few fonts of typed or printed material. However, no reading machines with true multifont recognition capabilities are as yet in productive operation, and no devices are as yet available which can read handwritten material with the degree of success that would be accepted in many tasks as a reasonable substitute for the human reader.

Today's data processing systems would be much more useful if they could accept a variety of printed, written, or graphic data as inputs. The symposium was arranged so that investigators working toward this end might benefit from knowledge of developments and findings in other laboratories. In addition, potential users were invited to attend to permit an interchange of information with respect both to requirements and to present-day capabilities. The information thus shared should facilitate development of new methods of optical character recognition and speed the day when more flexible input systems will become available for data processing.

The symposium was divided into two one-day and two half-day sessions. The first session featured talks on the characteristics of operative character recognition systems, given by people involved in developing them. The second session explored the trends in present character recognition research, while the third and fourth presented panel discussions on user requirements and the prospects for the future.

The symposium opened with a welcoming address by M. C. Yovits of ONR. The first session consisted of talks, under the chairmanship of D. K. Pollock of ONR, describing character recognition systems now in operation or being prepared for delivery in the near future. The first paper was by W. T. Hannan of Applied Research, Defense Electronics Products, RCA. He described the RCA multifont reading machine which uses interchangeable photographic matrix masks as reference patterns, accomplishes the recognition-decisions by means of optical correlation techniques, and incorporates automatic line and character location features in the electronic scanning system. A reading rate of 500 characters per second at accuracies of 1 to 5 errors per million characters was reported for this machine. Potential applications to the reading of printed pages, including Cyrillic texts, were discussed.

G. L. Fischer and C. C. Heasly, Jr. of Farrington Electronics were the co-authors of a paper which discussed optical scanning requirements with special reference to automatic input systems for a variety of applications. A new model Farrington reader, the Selected Data Page Scanner, was announced in a press release coinciding with the opening of the symposium. The new reader incorporates interchangeable plugboard-programming format-control features to facilitate line location and field location within a line and to accommodate various word length and storage mode conditions.

Following this paper, J. Rabinow described the several approaches to automatic character recognition that have been investigated by the Rabinow Engineering Company, Inc. Readers using varied techniques, including optical-mask coincidence correlation, weighted area matrix correlation, and multiple non-re-entrant curve tracing, were discussed. It was concluded that anything now typed or printed can be read by machine and that within 5 to 10 years, cursive handwriting should be machine readable.

J. B. Chatten and C. F. Teacher of the Philco Research Center next described the use of high resolution flying spot scan techniques in a variable-font address reader being developed for the Post Office Department. Features include automatic character location, means to normalize the size of unknown characters, following of lines regardless of tilt, and provisions for re-scanning to resolve ambiguity on a character-by-character basis. Recognition decisions in the Philco reader are based on shift-register correlations where the unknown pattern is compared with a number of weighted area reference patterns stored in the form of resistor arrays.

The principles of operation of a page-reader for Cyrillic text, under development by Baird-Atomic, Inc., were presented by J. A. Fitzmaurice. This reader uses an optical correlation technique for character recognition at rates up to 1000 characters per second. Input is in the form of microfilm copies of pages of printed Russian language material. Problems of handling special symbols, equations, and other interspersed graphic material were discussed.

The advantages of vidicon scanning techniques in character recognition systems using

an area analysis principle were discussed by P. Barth of the National Data Processing Corporation, a Division of Remington Rand UNIVAC. He described results of this technique as giving recognition rates of up to 1000 characters per second for 20-microsecond exposures of the source documents.

Leon Mintz described the typed page reader developed for the Army Signal Corps by the Control Instrument Division of Burroughs Corporation. This equipment was designed to read upper- and lower-case alphanumeric characters in standard elite type font. The device reads types pages stacked in its input hopper and converts the characters into teletype code at a rate of 75 characters per second. Line tilt of as much as 10 degrees can be accommodated without loss of reading accuracy.

A numeric character reader that will accept wide tolerances in quality of printing was described by R. K. Gerlach of the Electronics Division of the National Cash Register Company. The NCR equipment was designed for use with a special font; source documents consist of paper strips imprinted by various accounting and cash register machines. Reject rates of the order of 10^{-4} and error rates of 10^{-6} were reported for this equipment.

A paper by W. T. Booth, G. M. Miller, and O. A. Schleich described character recognition developments at the General Electric Company. A recently developed machine has been designed to read the numeric font under consideration by the X3.1 Subcommittee of the American Standards Association. Several recognition logics for reading at rates up to 2500 characters per second were described. Problems in reading misregistered and degraded characters were discussed.

The first day's session was concluded by E. C. Greanias of the Advanced Systems Development Division, IBM, who discussed various factors which affect the realization of practical character recognition devices. The nature of the documents to be read, the administrative control that can be exercised in document preparation, the costs of handling rejects, were discussed in terms of determination of economic feasibility. The progress made in the development of methods of pattern analysis was noted. The recognition logic, testing procedures, and printer evaluation studies used in the development of the IBM 1418 reader were described.

The second day's session was devoted to trends in character recognition research. The first speaker was A. B. Novikoff of the Mathematical Sciences Department, Stanford Research Institute. He discussed the need for a usable mathematical model for "geometric noise" which results from random disturbances of a pattern from its ideal representation. General requirements which such a model should satisfy and the example of a particular proposed model were described.

A system for reading cursive handwriting was described by L. D. Harmon of the Bell Telephone Laboratories. Two distinct problems are involved: The segmentation of the handwritten word into its component characters and the recognition of the script letters themselves. A system involving the use of local, criterial features has been developed and tested on sentences written with a special stylus under the constraints of observing base and guide lines. An accuracy of 90 percent was achieved with a number of samples from different writers. The use of confusion matrix statistics and diagram probabilities to improve performance was described.

A comparison of computed moments of input character patterns with the corresponding moments of prototype patterns was described by F. L. Alt of the National Bureau of Standards. He pointed out that certain combinations of moments are relatively invariant for pattern transformations such as size, translation, and some slanting. Experiments on a computer indicate that a process using a modest number of sample points and computing moments only up to the sixth order is adequate to discriminate between the characters of a given alphabet. The general problem of classifying items characterized by a set of numbers was discussed.

The next paper, by R. F. Meyers, V. E. Giuliano, and P. E. Jones of Arthur D. Little, Inc., similarly postulated sets of mathematical derivatives of certain integral measurements of character patterns. It was noted that methods based on measurements of a number of moments or a number of Fourier coefficients offer means to normalize by computing a set of invariants with respect to frequently encountered pattern transformations, such as translation or scaling. A procedure was described for obtaining a set of measurement functions which minimize the error rate for a given alphabet and a given degree of noise.

D. M. Baumann of the Massachusetts Institute of Technology described preliminary results of a study of the use of area weighting techniques for automatic character recognition. Input character patterns were categorized into subsets on the basis of optical sensing through a sequence of photographic masks. Mask design was based upon statistical parameters of a set of characters and weighting functions chosen to provide optimal separation.

A paper by L. G. Roberts reviewed character and pattern recognition developments at the Massachusetts Institute of Technology during the past 5 years. It was noted that earlier research on handprinted characters was followed by studies on cursive handwriting and that progress has been made in characterizing handwritten strokes.

Continuing pattern recognition research in the general Perceptron research program was reported in a paper by W. S. Holmes, H. R. Leland, and J. L. Muerle of the Cornell Aeronautical Laboratory. In particular, a multilayered Perceptron system has been simulated by computer to investigate the feasibility of training the system to recognize mixed font alphanumeric characters. The input pattern is prefiltered to provide a transformed image space, combinations of intensities at selected points in the transformed image space are used as properties, and a linear discriminant function is applied to classify the pattern.

A scheme for recognizing patterns from an unspecified class was described by C. Barus of Swarthmore College. Small subsets of specimens of each of the patterns to be recognized are stored in the machine. The information contents of these subsets change during a learning phase to become more typical of the pattern represented. Possibilities for implementation by optical comparisons were discussed.

In a paper by W. H. Highleyman of the Bell Telephone Laboratories, a distinction was made between the "receptor" and the "categorizer" operations of a pattern recognition system. The categorizer typically determines, from measurements made by the receptor on an unknown pattern, the particular pattern class to which the unknown belongs. The paper considered in detail that class of categorizers involving the linear decision functions. In connection with the problem of recognizing handprinted numeric characters, procedures were illustrated based upon sampling from pattern classes to be identified for choice of linear decision function.

Techniques for multifont print recognition were described by M. C. Andrews of the Thomas J. Watson Research Laboratory of IBM. Problems encountered and experimental techniques which offer apparently promising solutions were discussed. The speaker also described automatic error detection and correction methods applicable to systems which are required to accept and process natural language text.

M. B. Clowes of the National Physical Laboratory, Teddington, England, described a method for character recognition involving one or more autocorrelation functions of an unknown pattern. The form of the autocorrelation function specifies a character feature, such as a straight line or a "hook." Such functions are invariant with respect to transformations of size, rotation, and translation and are relatively insensitive to minor changes in style or printing quality.

L. Uhr of the University of Michigan presented a paper, prepared by himself and C. Vossler of the Systems Development Corporation, reviewing current trends in the "search to recongize." He noted the specific problems to be solved – the array differing with selections of font and vocabulary size, method of presentation, and method of recognition. It was also noted that, on the other hand, general methods for pattern recognition would allow for common solutions to families of problems. He then described a specific experimental technique which enables an adaptive categorization of information-carrying features of unknown inputs. Results were given for subsequent recognition both of hand-drawn alphanumeric characters and of certain outline drawings, including comic-strip faces.

The third session of the symposium consisted of a description and panel discussion of representative user requirements in various government agencies. The panel was under the chairmanship of B. Radack, Bureau of Supplies and Accounts, Navy, and was composed of G. Shiner, Rome Air Development Center; C. Sparks, U.S. Civil Service Commission; P. Howerton, Central Intelligence Agency; Major L. Sears, Army Finance Office; R. Hessinger, Post Office Department; and W. Velander, Navy Management Office.

The fourth and final session was held Wednesday afternoon, 17 January, under the chairmanship of M. C. Yovits of the Office of Naval Research. This session was opened by a

keynote address by O. G. Selfridge of the Massachusetts Institute of Technology. The following panel discussion brought forth remarks on the horizons for optical character recognition research by J. D. Noe, Stanford Research Institute; J. C. R. Licklider, Bolt, Baranek, and Newman; H. A. Affel, Jr., Auerbach Corporation; D. H. Shepard, Cognitronics; D. Brick, Sylvania; and J. J. Eachus, Minneapolis-Honeywell.

A Proceedings will be available, in September 1962, at an approximate price of $10.00. The publisher is Spartan Books, 6411 Chillum Place, Washington 12, D. C., and orders should be directed to Spartan Books or to a bookstore.

PLATO II—UNIVERSITY OF ILLINOIS, URBANA, ILLINOIS

Introduction

The purpose of the PLATO (Programmed Logic for Automatic Operations) project is to develop an automatic teaching system capable of tutoring simultaneously a large number of students in a variety of subjects. The central control element of the teaching system is a general purpose digital computer. The PLATO system differs from most teaching systems in that a single high-speed digital computer is used to control all student stations. Thus, it has available the power of a large digital computer to teach each student. A complete description of the equipment and systems organization was described in the April 1962 issue of DCN.

Teaching Studies with College Undergraduates

A study was completed in which PLATO II was used to teach the first week of the University's course "Introduction to Automatic Digital Computing (Math 195)." This course uses the IBM-650 as a vehicle for introducing the student to the basic notions of automatic computing.

On the first day of class, some 20 students were chosen at random and asked to attend a demonstration of the machine. After the demonstration, nine volunteers were found whose schedules were compatible with our schedule for use of the computer. These nine students formed the subjects of our study.

Each student was first given a practice session (with specially prepared material) to familiarize him with the operation of the machine. These practice sessions reconfirmed our previous experiences that students could master the operation of the machine in a few minutes. No student reported any difficulty in this respect, either during the practice session or the lessons proper.

Each student was then scheduled for three lessons on the machine. Since these lessons paralleled, almost exactly, the subject-matter discussed by the instructor in class, the students were encouraged not to attend class for the week of the study. None did.

Topics covered by the three lessons were:

Lesson 1: The Word as a Number (fixed and floating point representation)

Lesson 2: The Biquinary Code and the Storage Unit

Lesson 3: The Arithmetic Unit, Instruction Format, the Control Unit, and Execution of Single Instructions.

Since the PLATO II system can teach two students simultaneously, the students were, when possible, scheduled in pairs so that the nine students each taking the three lessons represent roughly 15 hours of scheduled computer time.

The records kept by the computer during each run of each student's progress through the material are currently being studied. The results and conclusions will be available shortly for publication. The data collected provides information about:

1. The learning ability of each student.

2. The effectiveness of each lesson.

3. The data rate requirement placed on the system.

More specifically, under each item the following kinds of information are available.

1. Student

   a. length of time the student spent on each lesson

   b. number of times the student requested help

c. number of wrong answers submitted by the student.

2. Lesson

   a. average length of time spent on each slide.

   b. problems of the main sequence for which heop was requested

   c. problems for which the computer was requested to supply the correct answer by the student.

3. System

   a. average rate of inputs to central computer (per unit time per student)

   b. number of times each type of request was entered into the computer (e.g., continue, judge, etc.).

Some data may be of significance in more than one of the above categories, nor is the above list intended to be exhaustive. It does give a fair sample of the type of data available from a study with PLATO II.

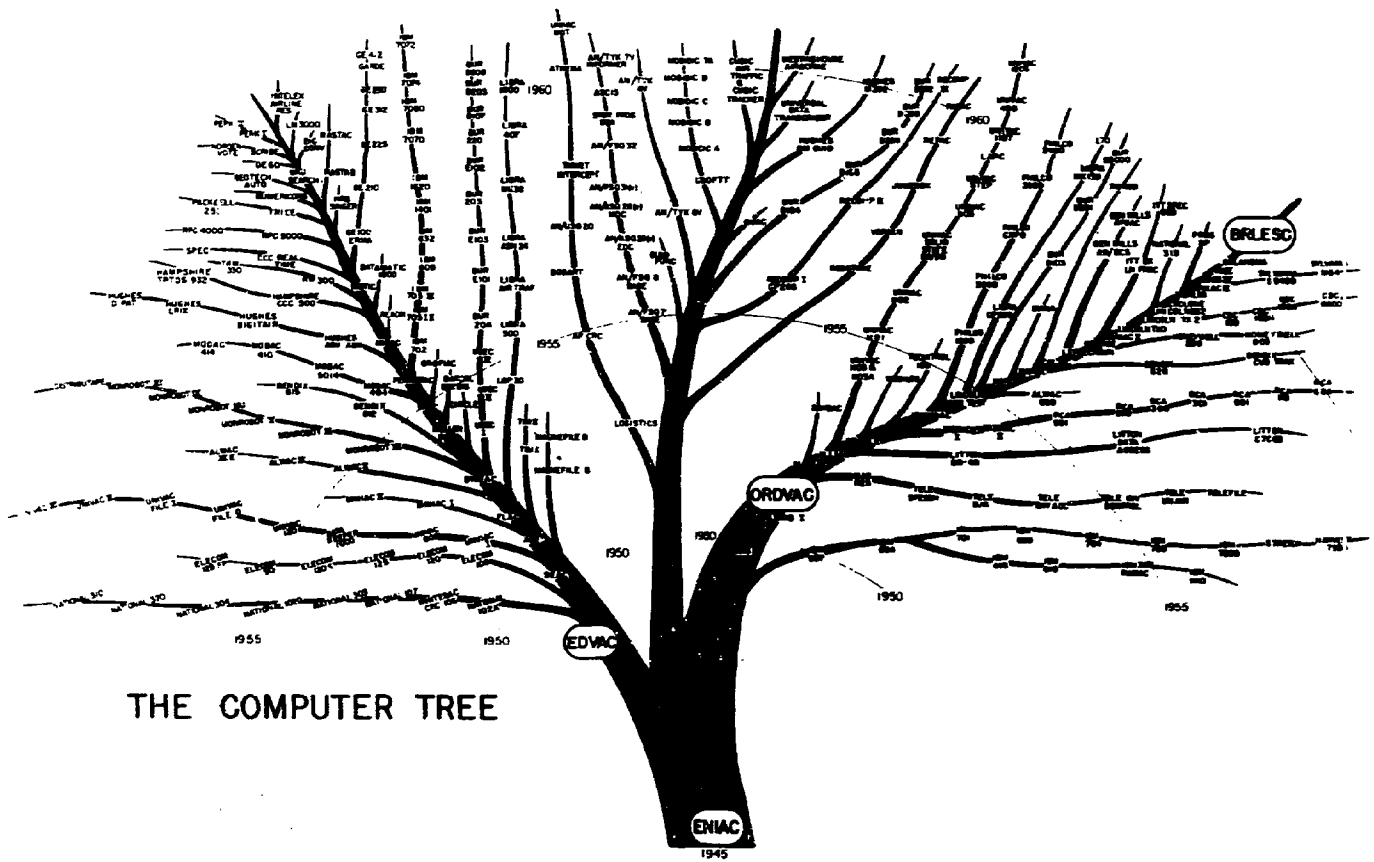
At the end of the third week of the course, the instructor gave the class an examination covering both material taught with the machine and later material taught only in class. The average grade on this examination of the students who had participated in the study was almost precisely equal to the class average as a whole.

Finally, we should like to report that all students, at least for the week of the study, seemed enthusiastic about the machine. None indicated any desire to drop out, although they were reminded several times that they could do so.

THE COMPUTER TREE—U.S. ARMY BALLISTIC RESEARCH LABORATORIES COMPUTING LABORATORY, ABERDEEN PROVING GROUND, MARYLAND

The automatic data processing industry is a direct outgrowth of Army sponsored research, which produced ENIAC, the first modern electronic computer, in 1945. The computer industry has grown to a multi-billion dollar activity, and has penetrated every profession and trade in Government, business, industry, and education. The Computer Tree shows the evolution of computers. The serial computers, represented by the EDVAC, and the parallel computers, represented by the ORDVAC, are shown as separate trunks. This has also tended to separate the slower business computers from the faster scientific computers. Military requirements have fostered a central composite shoot and have stimulated other growths. Manufacturers have entered the computer field at different times, producing various branches along the main bough. The radial distance from the ENIAC is an approximate indication of the year each computer was either developed, constructed, or placed in operation.

The ENIAC, EDVAC, ORDVAC, and BRLESC were sponsored or developed by the Ballistic Research Laboratories, Aberdeen Proving Ground, Maryland (see other BRL article, this issue of DCN).



THE COMPUTER TREE